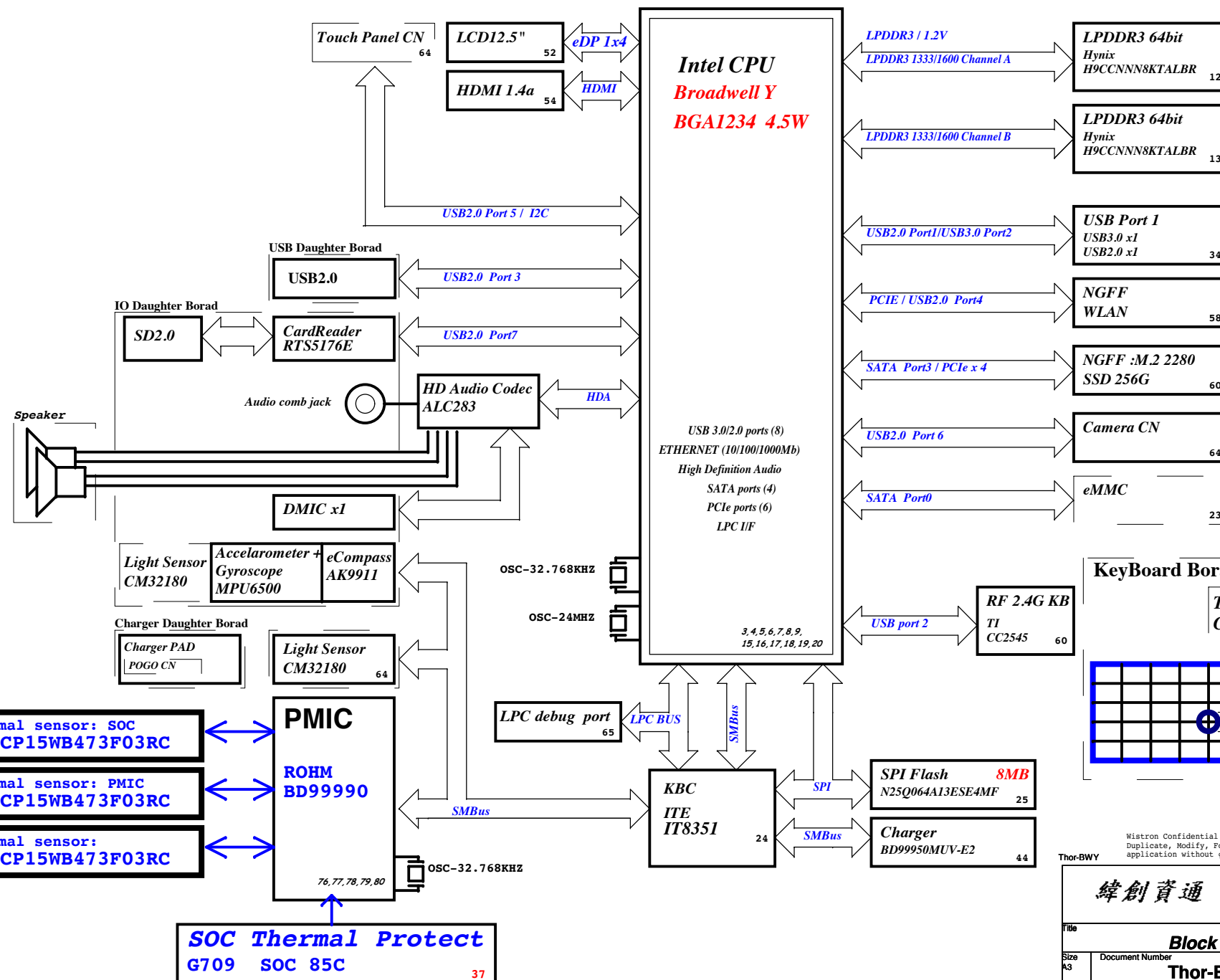


Thor-BWY Block Diagram

Project code : 4PD03E010001

PCB P/N : 14210

Revision : -1



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Thor-BWY

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Block Diagram		
File	Document Number	Rev
Size A3	Thor-BWY	-1
Date: Tuesday, August 12, 2014	Sheet 1 of 102	

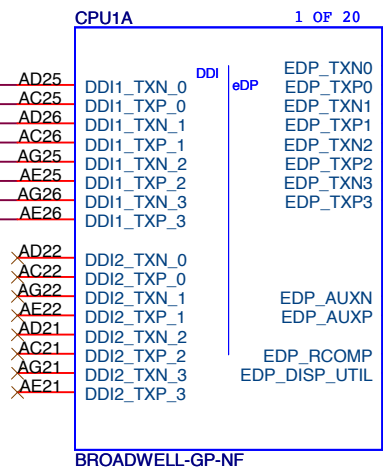
Thor-BWY 2014-09-01 REV : -1

SA Setting	Dummy		SA Setting	Dummy		SD Setting	Dummy		SA Setting	Dummy	
V	NON_DS3		V	INTVR_EN		V	TOUCH_I2C		V	PMIC_AC_OK	
	DS3			EXTVR_EN			TOUCH_USB			CHG_AC_OK	
SA Setting	Dummy		SA Setting	Dummy		SA Setting	Dummy		-1 Setting	Dummy	
V	NON_CS			PMIC_ADC_VREF			POGO_KB			KBC_BLEN	
	CS		V	ADC_VREF		V	2.4G_KB		V	CPU_BLEN	
SA Setting	Dummy		SA Setting	Dummy		SA Setting	Dummy				
V	NON_M		V	PMIC_EC_RST			PMIC_RTC_CLK				
	M			RC_EC_RST		V	SOC_RTC_CLK				

SSID = CPU

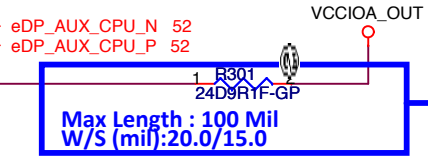
HDMI

54 HDMI_DATA_CPU_N2
54 HDMI_DATA_CPU_P2
54 HDMI_DATA_CPU_N1
54 HDMI_DATA_CPU_P1
54 HDMI_DATA_CPU_N0
54 HDMI_DATA_CPU_P0
54 HDMI_DATA_CPU_N3
54 HDMI_DATA_CPU_P3



AD17
AC17
AG18
AE18
AD18
AC18
AA17
W17

eDP



Layout Note:

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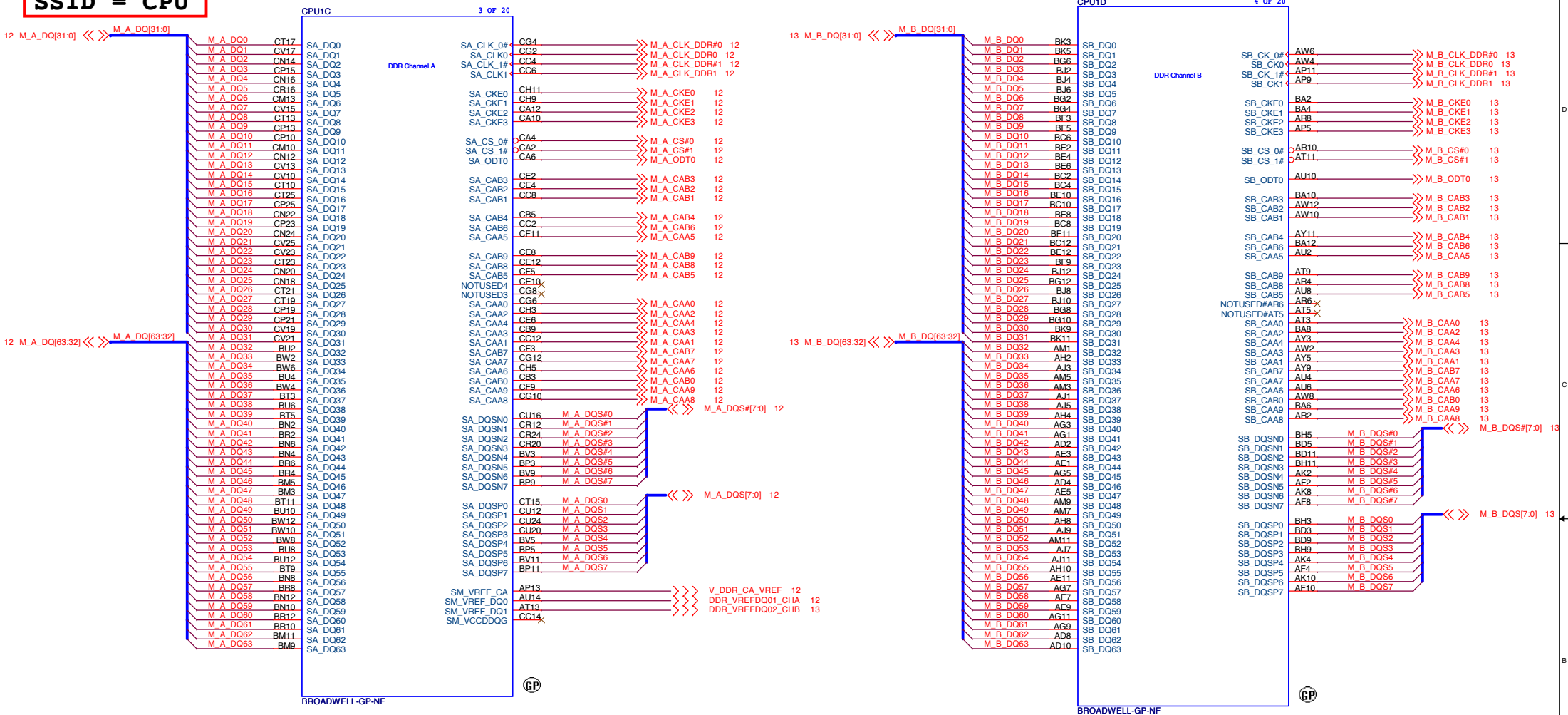
Thor-BWY

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Title			
MCP CPU(DDI/EDP)			
Size	Document Number	Rev	
A4		-1	
Date:	Monday, August 18, 2014	Sheet	3 of 102

E



SSID = CPU



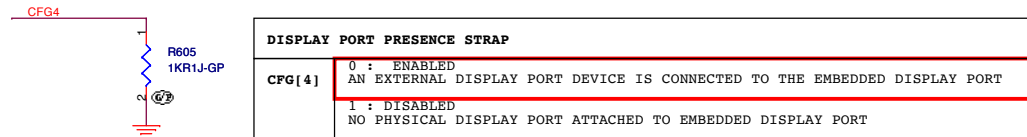
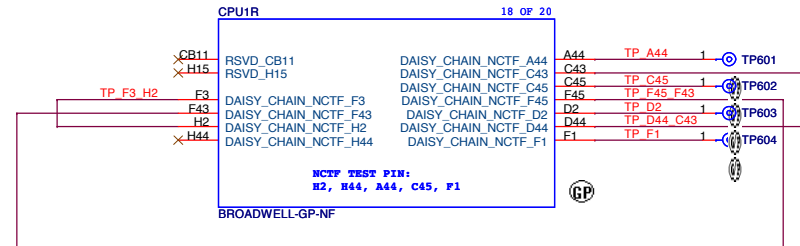
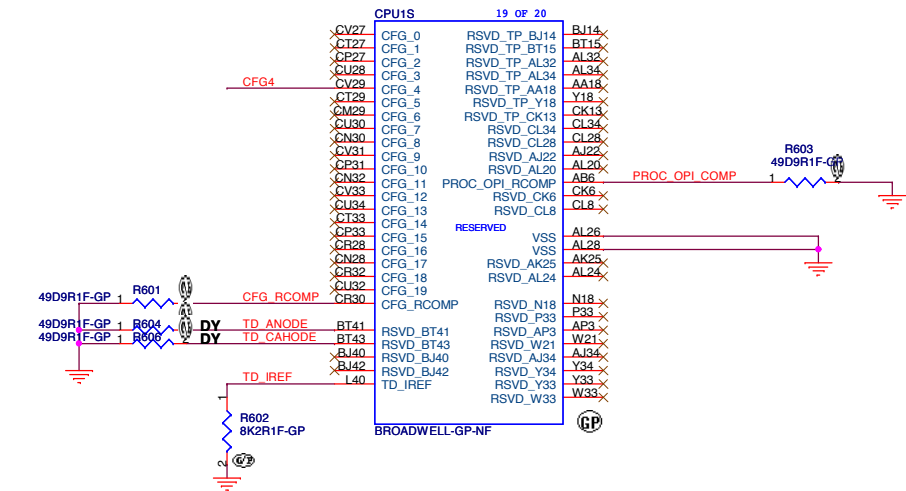
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Title			
MCP CPU(DDR)			
Size A3	Document Number		Rev
	Thor-BWY		-1
Date:	Monday, August 18, 2014		Sheet 5 of 102

SSID = CPU



DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT
	1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

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Thor-BWY

File		CPU (RESERVED)	
Size	Document Number	Rev	
A3	Thor-BWY	-1	
Date:	Tuesday, August 12, 2014	Sheet	6 of 102

SSID = CPU

Layout Note:

Layout Note:

76_VR_SVID_ALERT#
76_H_CPU_SVIDCLK
76_H_CPU_SVIDDAT
4.78_H_VCCST_PWRGD
76_H_VR_EN_CPU
76_H_VR_READY_CPU

Layout Note:

Layout Note:

NEAR PINS AJ20

NEAR PINS AJ20

CPU1L 12 OF 20

RSVD_CJ32 VCC_BK45
RSVD_CM33 VCC_CB41
CT3 VCC_CA40
CY3 VCC_BY41
CB1 VCC_BW40
BV1 VCC_CY17
CF1 VCC_AY45
BA14 VCC_BB45
CL1 VCC_BD45
CM3 VCC_BF45
CW1 VCC_BH45
AP1 VCC_BT45
AV1 VCC_BV45
BB1 VCC_BY45
BC14 VCC_CB45
BE14 VCC_CD45
BF1 VCC_CF45
BK1 VCC_CM45
BP1 VCC_CN44
CR1 VCC_CR43
AV45 VCC_CV43
RSVD_CJ28 VCC_CV45
CH45 VCC_CV19
AL16 VCC_CV21
AM43 VCC_CV23
AR40 VCC_CV25
AL22 VCC_CV27
AK33 VCC_CV29
CL14 VCC_CV31
CD43 VCC_CV33
CD43 VCC_CV36
CE40 VCC_CV38
BU14 VCC_CV42
CE42 VCC_CV44
CE43 VCC_CV45
CF39 VCC_CV46
CK40 VCC_CV47
CJ20 VCC_CV48
CJ22 VCC_CV49
CK23 VCC_CV50
CL26 VCC_CV51
CK27 VCC_CV52
CL22 VCC_CV53
CK21 VCC_CV54
RSVD_CL22 VCC_CV55
CK25 VCC_CV56
CM27 VCC_CV57
CK19 VCC_CV58
CJ16 VCC_CV59
CK31 VCC_CV60
AJ20 VCC_CV61

VCC_CORE

BK45
CB41
CA40
BY41
BW40
CY17
AY45
BB45
BD45
BF45
BH45
BT45
BV45
BY45
CB45
CD45
CF45
CM45
CN44
CR43
CR45
CU44
CV43
CV45
CY19
CY21
CY23
CY25
CY27
CY29
CY31
CY33
CY36
CY38
CY42
CY44
BM45
BP45
CA44
BV41
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BW44
CY40
CY13
CY15
BW42
BY43
CA42
CB43

BROADWELL-GP-NF

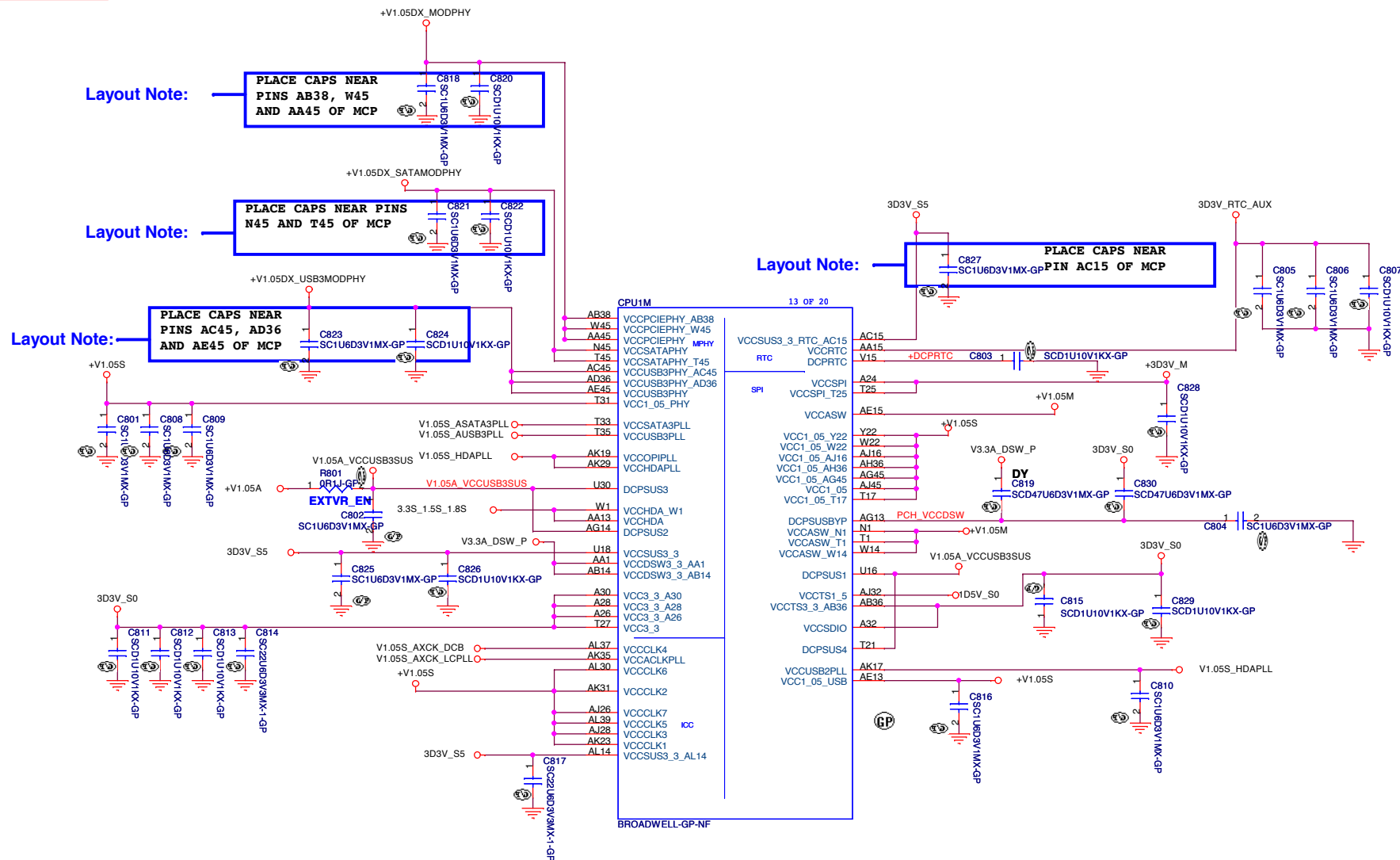
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Title			MCP CPU(VCC)	
Size	Document Number	Rev		
A3	Thor-BWY	-1		
Date:	Wednesday, August 20, 2014	Sheet	7	of 102

SSID = CPU



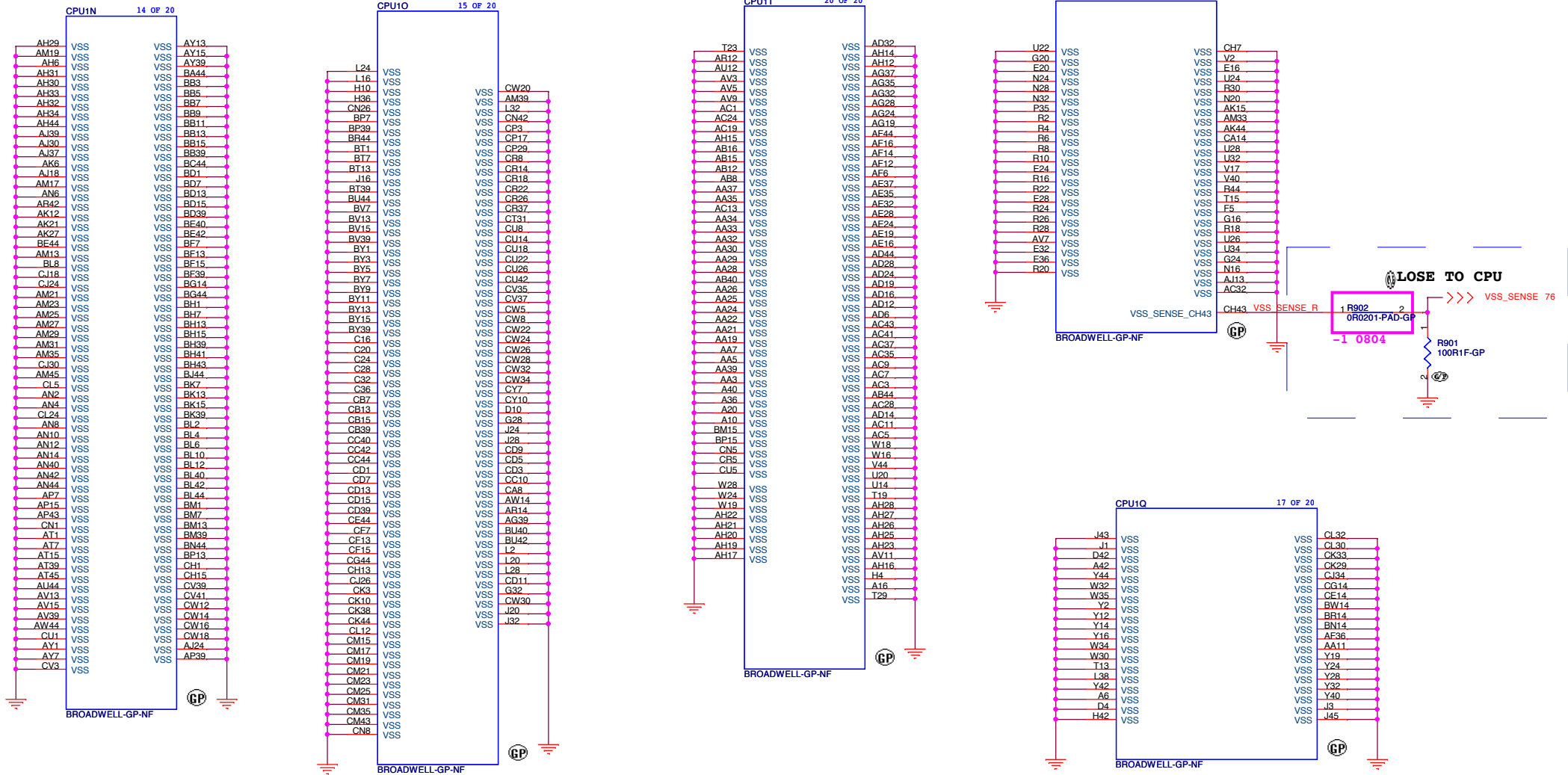
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Thor-BW Y

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Title			
MCP CPU(PWR1)			
Size A3	Document Number		Rev
	Thor-BWY		-1
Date:	Tuesday, August 12, 2014	Sheet 8 of	102

SSID = CPU

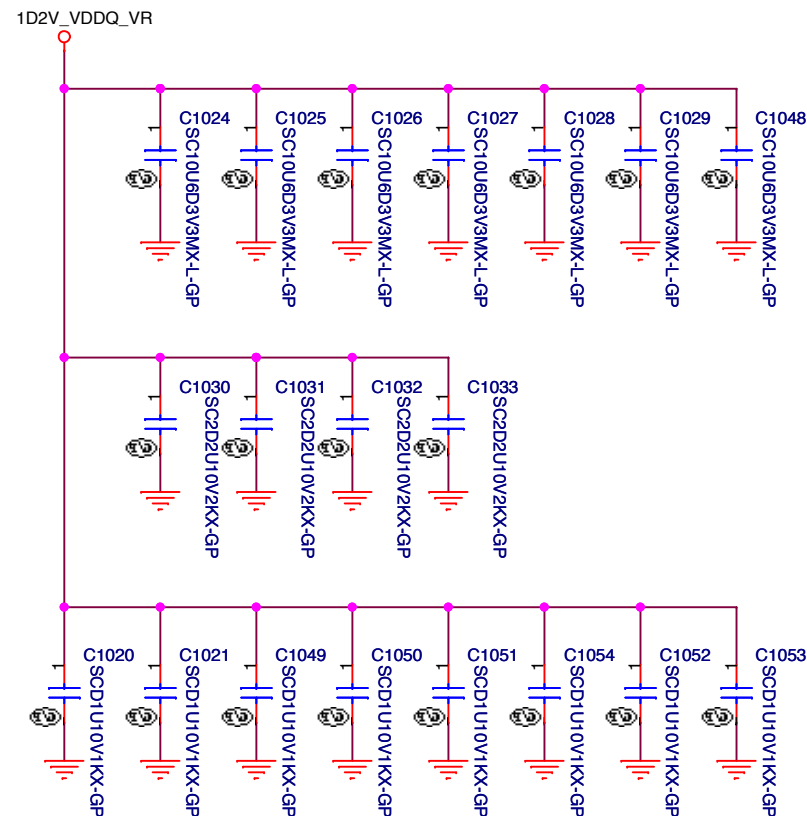
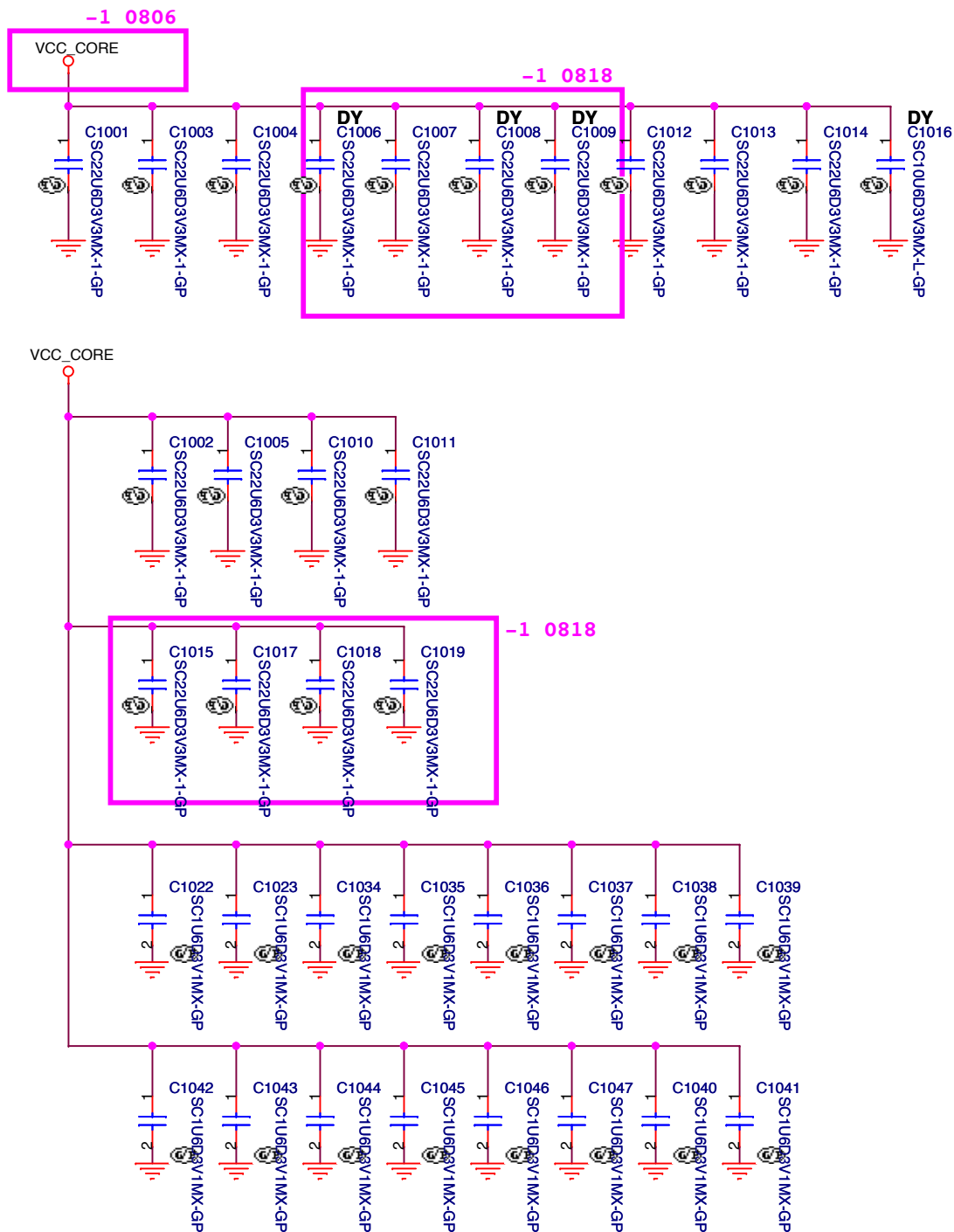


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Title		MCP CPU(VSS)	
Size	Document Number	Rev	
A3	Thor-BWY	-1	
Date:	Monday, August 18, 2014	Sheet	9 of 102

SSID = CPU Cap1



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Thor-BWY

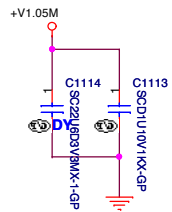
緯創資通

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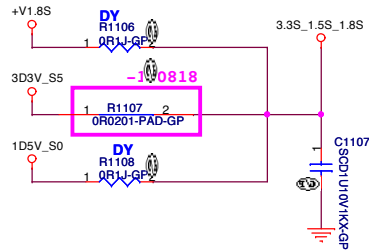
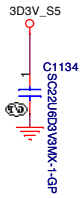
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title			CPU (Power CAP1)	
Size	Document Number		Rev	
A4	Thor-BWY		-1	
Date:	Monday, August 18, 2014		Sheet 10 of 102	

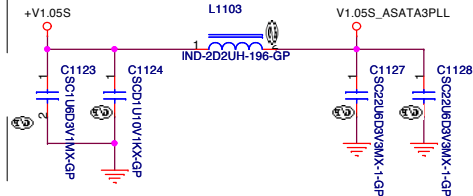
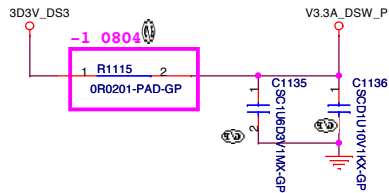
SSID = CPU Cap1



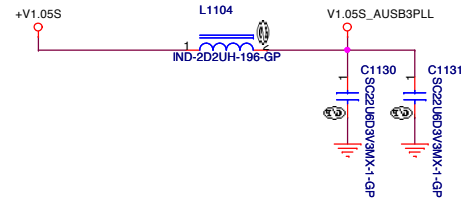
Place CAPS near PIN N1,T1,W14 of MCP



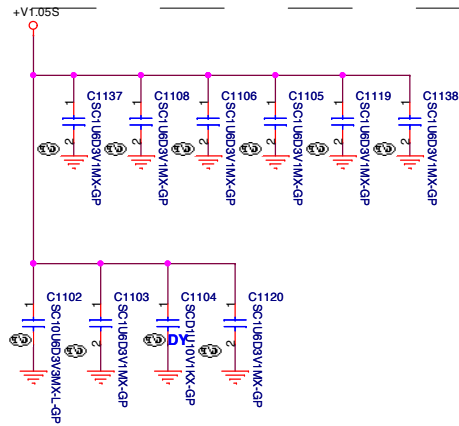
VCCHDA may be designed or configured to support two modes; HD Audio or 12S. If the circuit is designed and configured for HD Audio VCCHDA should be connected to 3.3V or 1.5V. If the circuit is designed and configured for 12S VCCHDA should be connected to 1.8V or 3.3V.



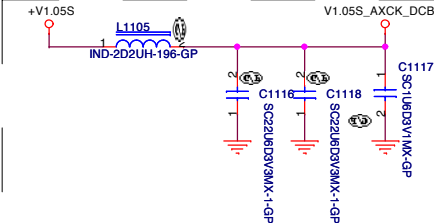
Place CAPS near MCP



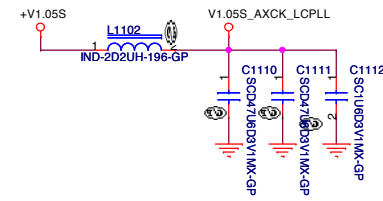
Place CAPS near MCP



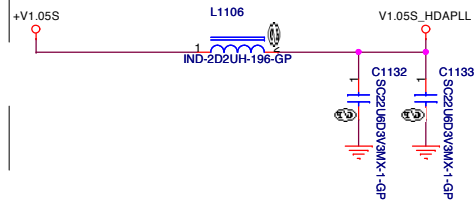
Place CAPS near MCP



PLACE CAPS NEAR PIN AL37 OF MCP



PLACE CAPS NEAR PIN AK35 OF MCP



Place CAPS near MCP

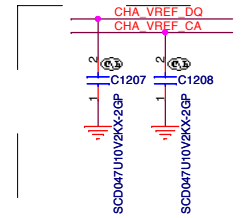
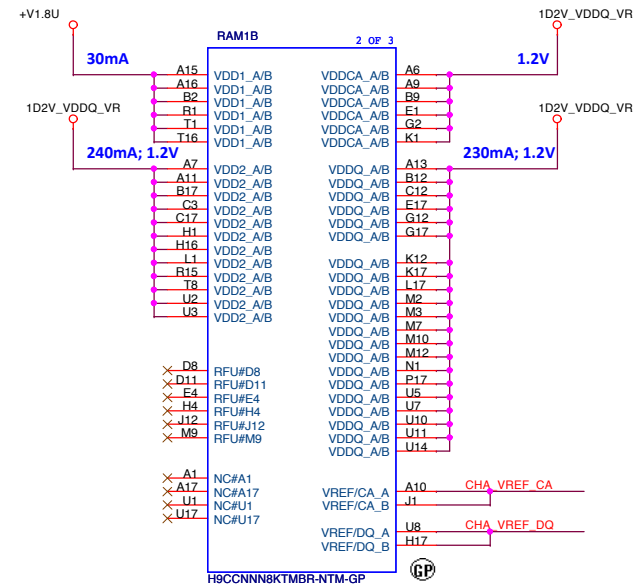
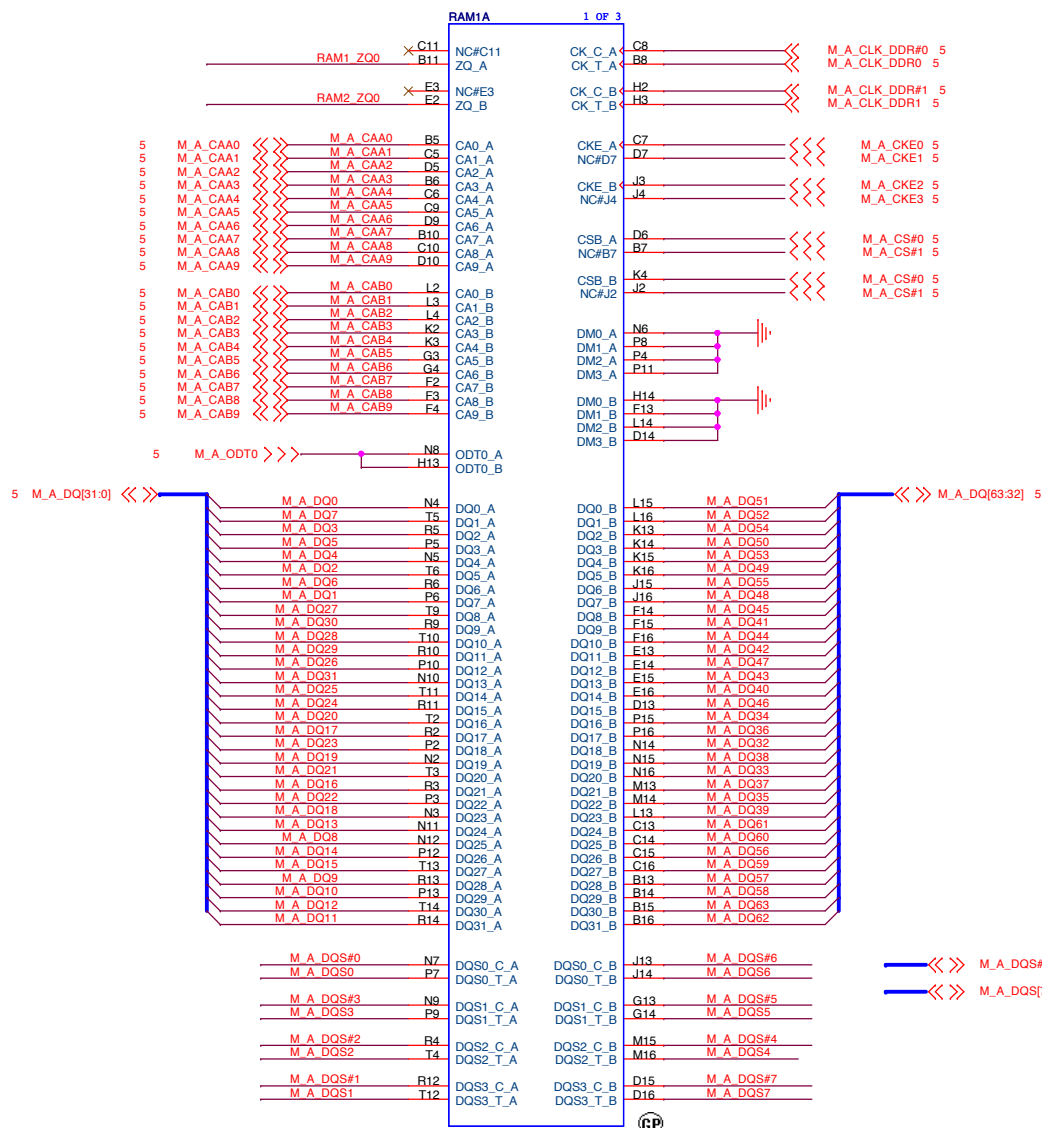
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Thor-BWY

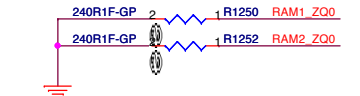
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Title			CPU (Power CAP2)	
Size	Document Number		Rev	
A3	Thor-BWY		-1	
Date:	Monday, August 18, 2014		Sheet	11 of 102

SSID = MEMORY



LPDDR3 CLK TERMINATION for layout: close to RAM1



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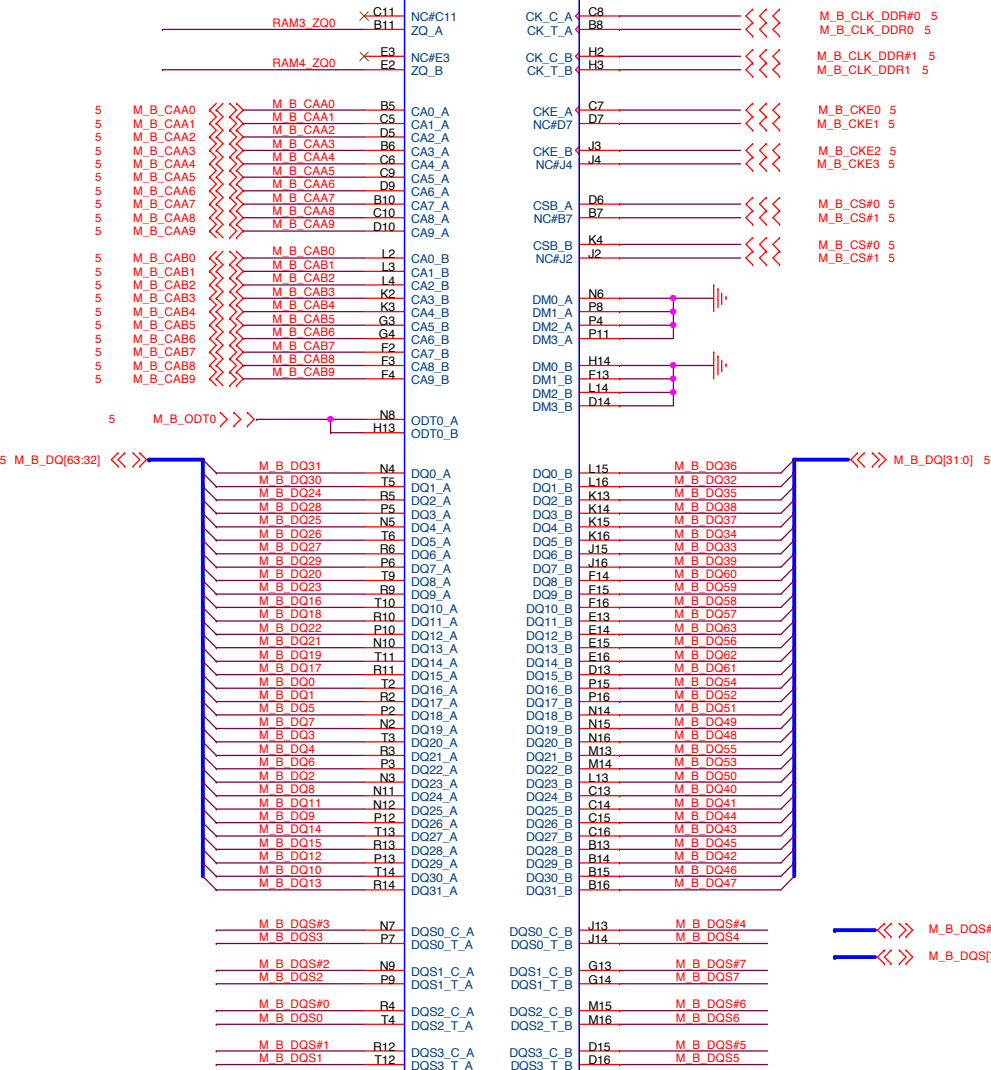
緯創資通 Wistron Corporation
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Thor-BWY

SSID = MEMORY

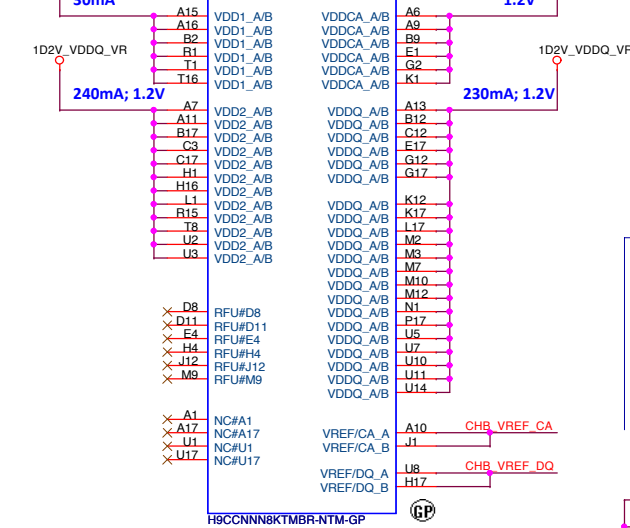
RAM2A

1 OF 3



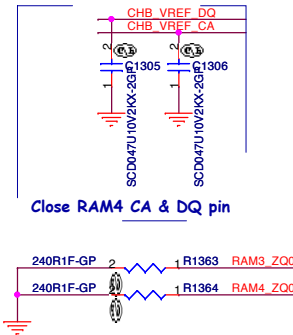
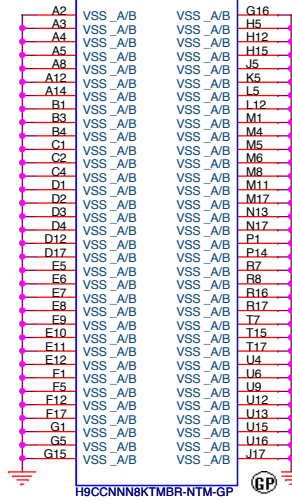
RAM2B

2 OF 3

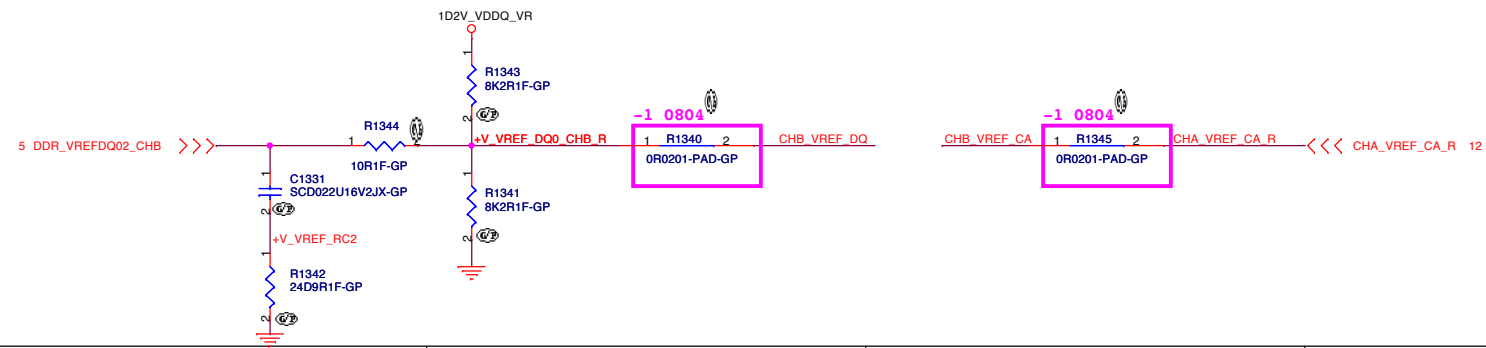


RAM2C

3 OF 3

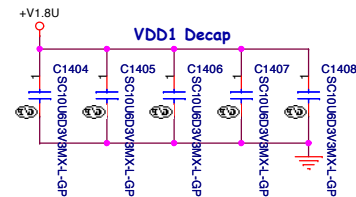
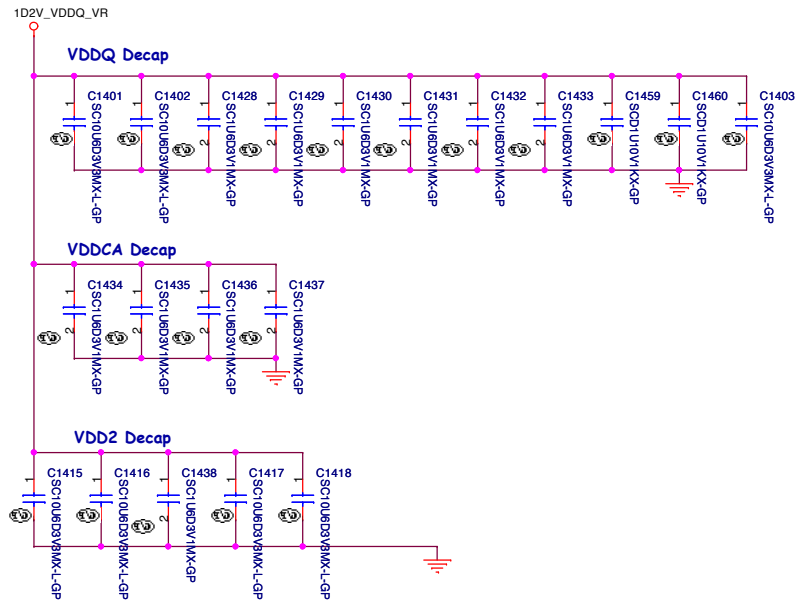


LPDDR3 CLK TERMINATION
for layout: close to RAM1

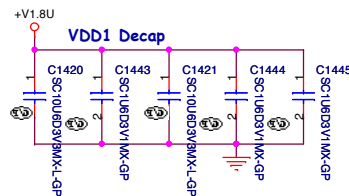
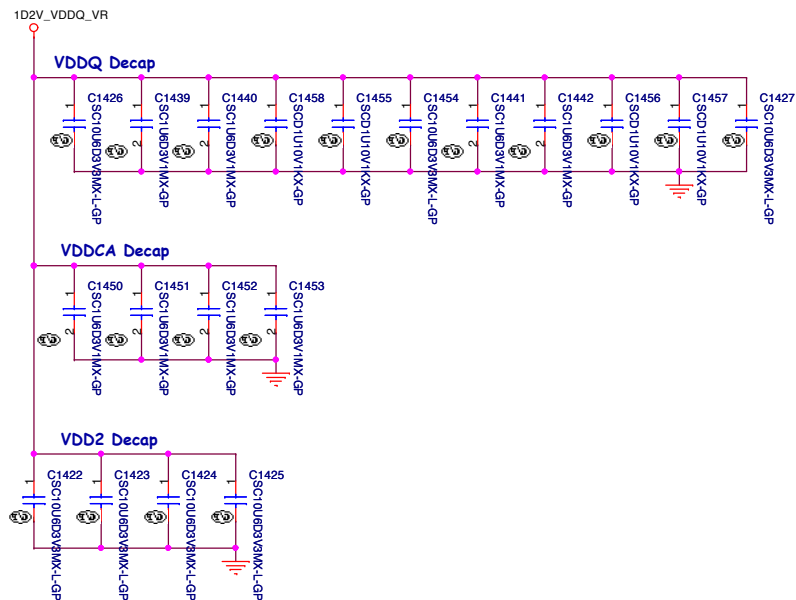


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SSID = MEMORY Cap



Layout Note:
Place these Caps near RAM



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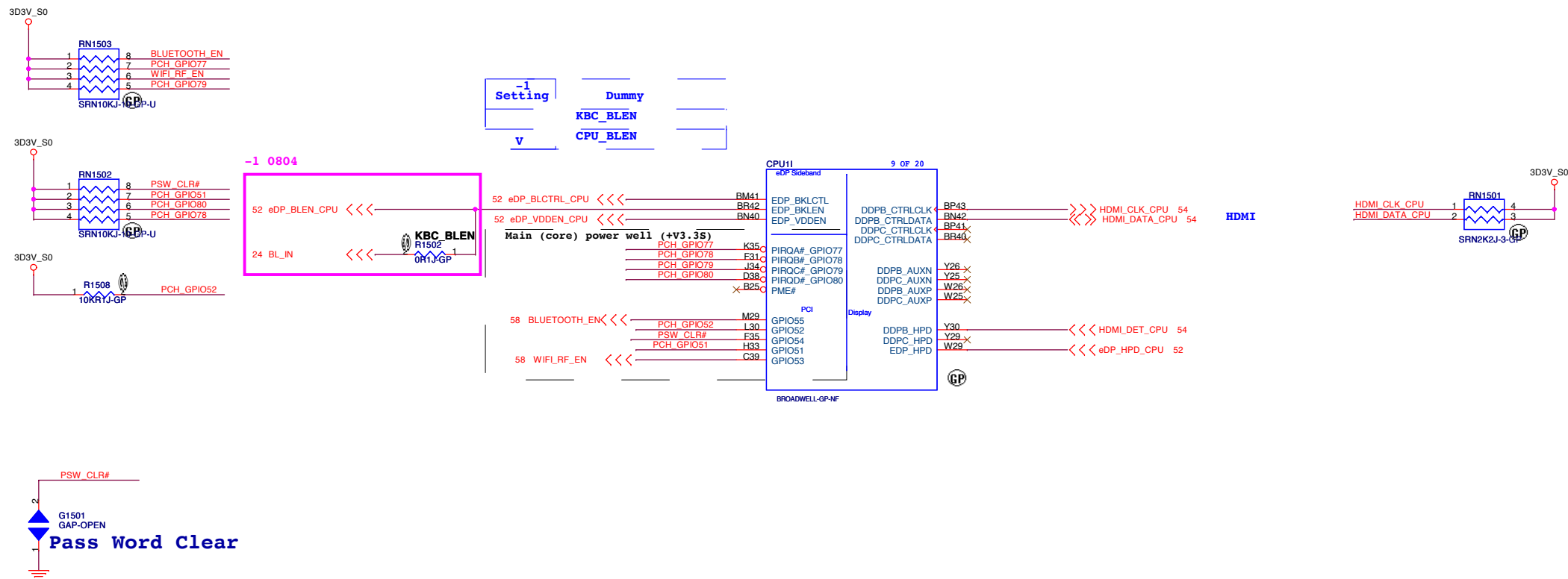
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Date:		Tuesday, August 12, 2014	
Document Number		LPDDR3(CAP)	
Rev		-1	
Sheet		14 of 102	

SSID = CPU

53.3.30GPIO Signals

All unused GPIOs, which are GPI by default should be pulled-up to their respective power wells through 8.2–10 K Ω resistor.



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Title

MCP PCH(EDP/GPIO/DDI)

Size	A3
------	----

Document Number

Thor-BWY

Rev	-1
-----	----

Date: Monday, August 18, 2014

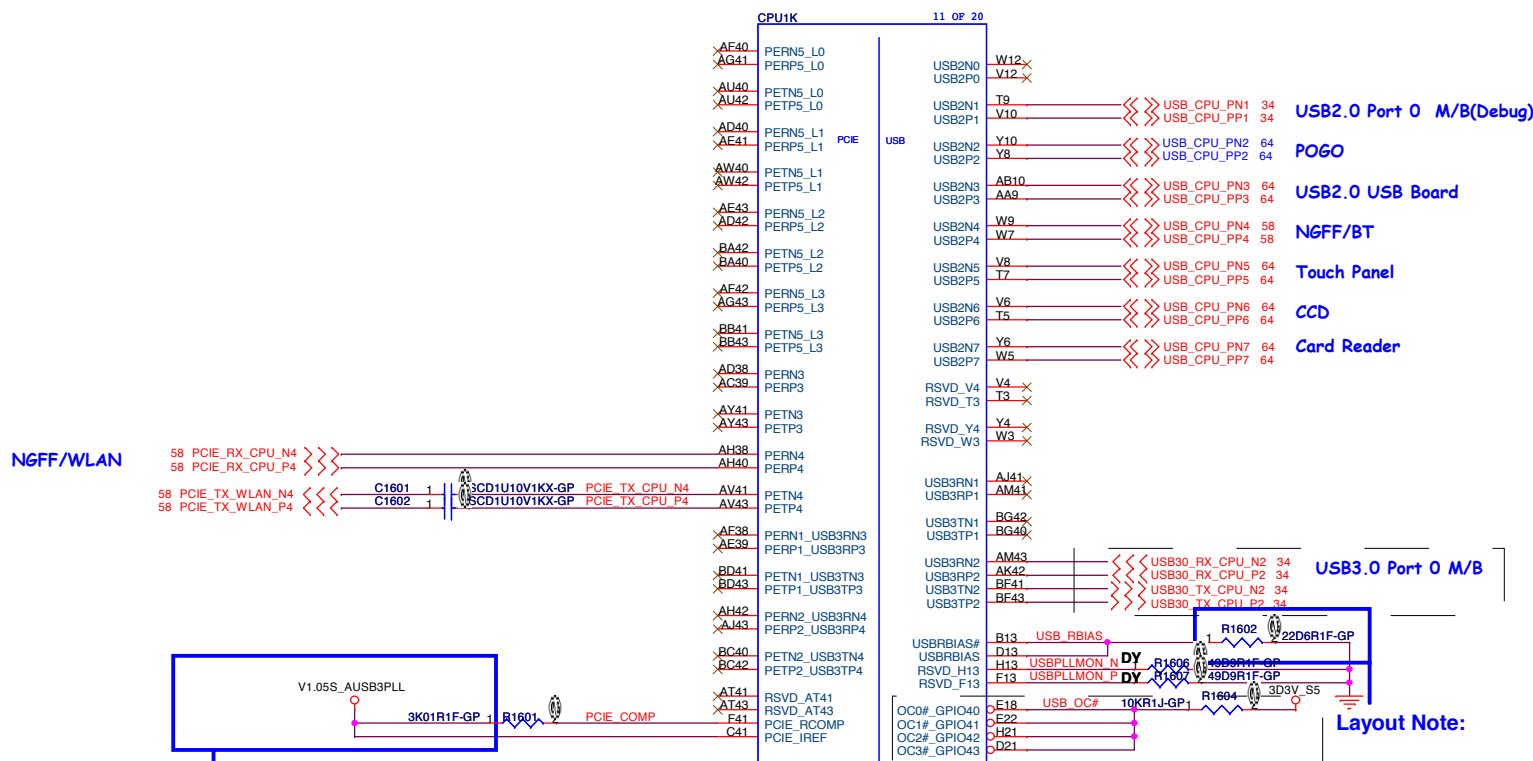
Sheet 1

102

SSID = PCH

USB Table

Pair	Device
0	
1	USB3.0 Port1
2	POGO
3	USB2.0 Port2
4	BT
5	Touch Panel
6	CCD
7	Card Reader



Layout Note:

1. PCIE_RCOMP/PCIE_IREF trace width=12-15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
PCIE_RCOMP	4 mils min (breakout) 12-15 mils (trace) Note: Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	3k ohm ±1% pulled to VCCUSB3PLL.	Max total = 500 mils
PCIE_IREF	4 mils min (breakout) 12-15 mils (trace) Note: Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	No resistor. Must connect directly to VCCUSB3PLL.	Max total = 500 mils

Resume (SuS) well (VccSus_3 power-rail)

1. USB COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

USBRBIAS/USBRBIAS# Connection Guidelines

- Short the USBRBIAS and the USBRBIAS# pins at the package and then route on the top layer to one end of a 22.6 Ω ±1% resistor to ground (see Figure 15-2).
- Route signal using 50 ohm single-ended impedance and 500 mils (12.7-mm) max trace length and no longer than 450 mils to resistor.
- Avoid routing next to clock pins or under stitching capacitors. Recommended minimum spacing to other signal traces is 15 mils (0.381 mm).

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
PCIE_RCOMP	4 mils min (breakout) 12-15 mils (trace) Note: Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	3k ohm ±1% pulled to VCCUSB3PLL.	Max total = 500 mils
PCIE_IREF	4 mils min (breakout) 12-15 mils (trace) Note: Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	No resistor. Must connect directly to VCCUSB3PLL.	Max total = 500 mils

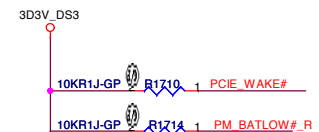
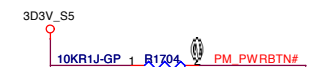
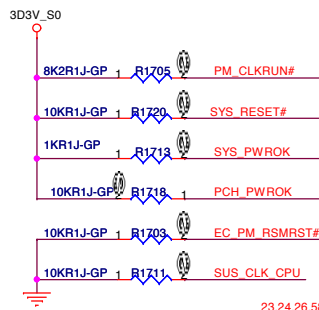
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Thor-BWY

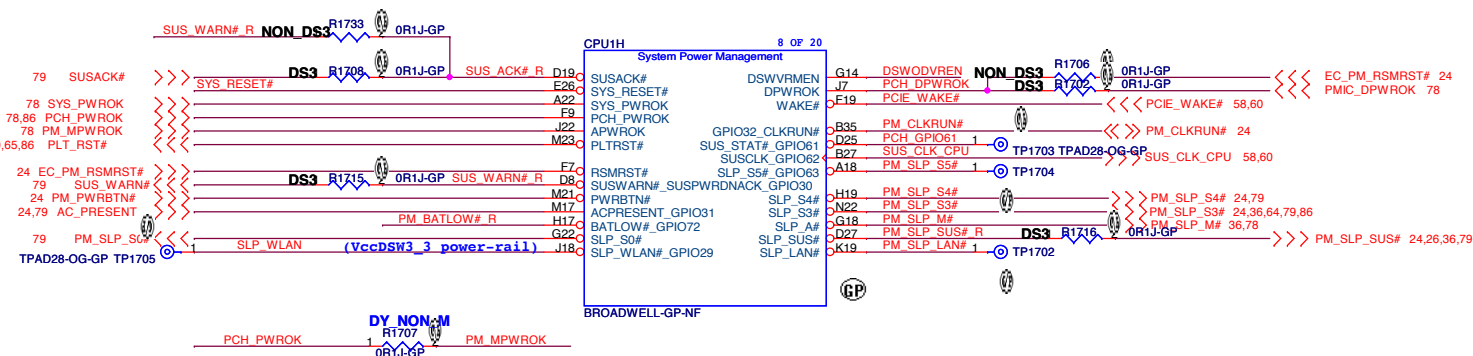
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Title			
CPU (PCIE/USB)			
Size A3	Document Number		Rev
Thor-BWY		-1	
Date:	Monday, August 18, 2014	Sheet 16 of	102

SSID = PCH



SA Setting	Dummy
V	NON_DS3
	DS3



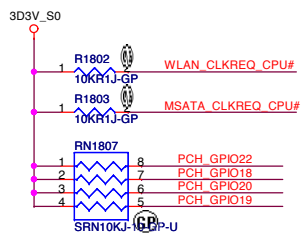
DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

Thor-BWY

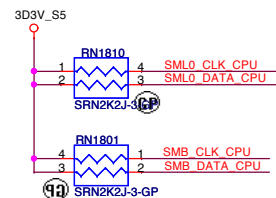
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File			
CPU (PM)			
Size A3	Document Number		Rev -1
Thor-BWY			
Date:	Wednesday, August 20, 2014	Sheet 17 of	102

SSID = PCH



Close to PCH

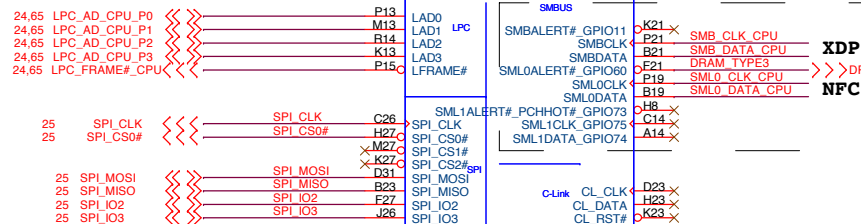
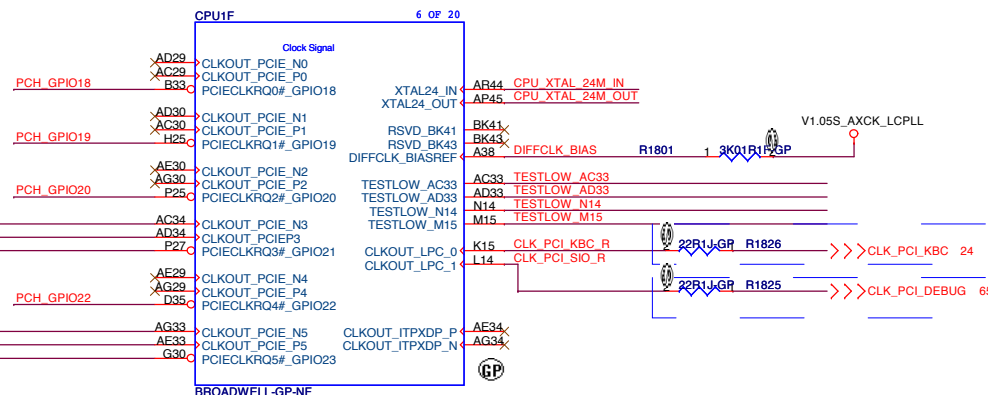


WLAN

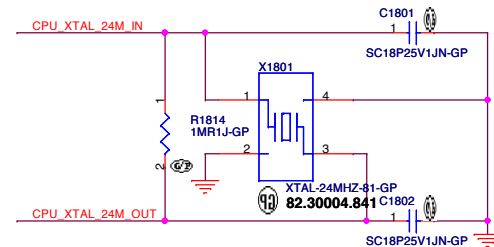
58 WLAN_CLK_CPU#
58 WLAN_CLK_CPU
58 WLAN_CLKREQ_CPU#

NGFF

60 MSATA_CLK_CPU#
60 MSATA_CLK_CPU
60 MSATA_CLKREQ_CPU#

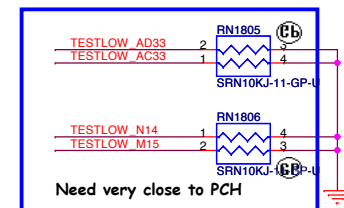


Resume (SuS) well
(VccSus3_3 power-rail)



LPC CLOCK CAN FEED ONLY 1 LOAD AT A TIME

CAN ONLY HAVE PORT80 OR TPM.
LOAD ONE REISTOR OR THE OTHER



Need very close to PCH

Layout Note:

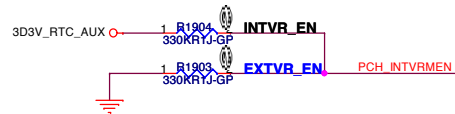
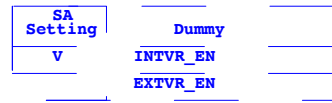
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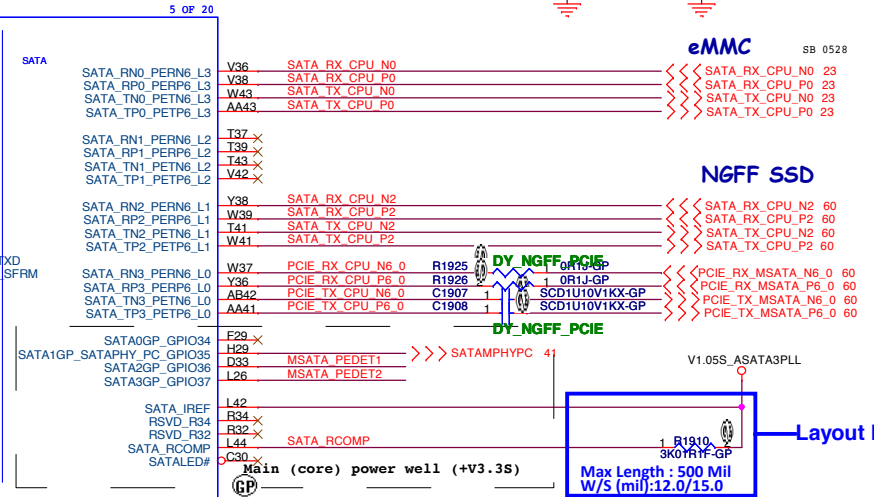
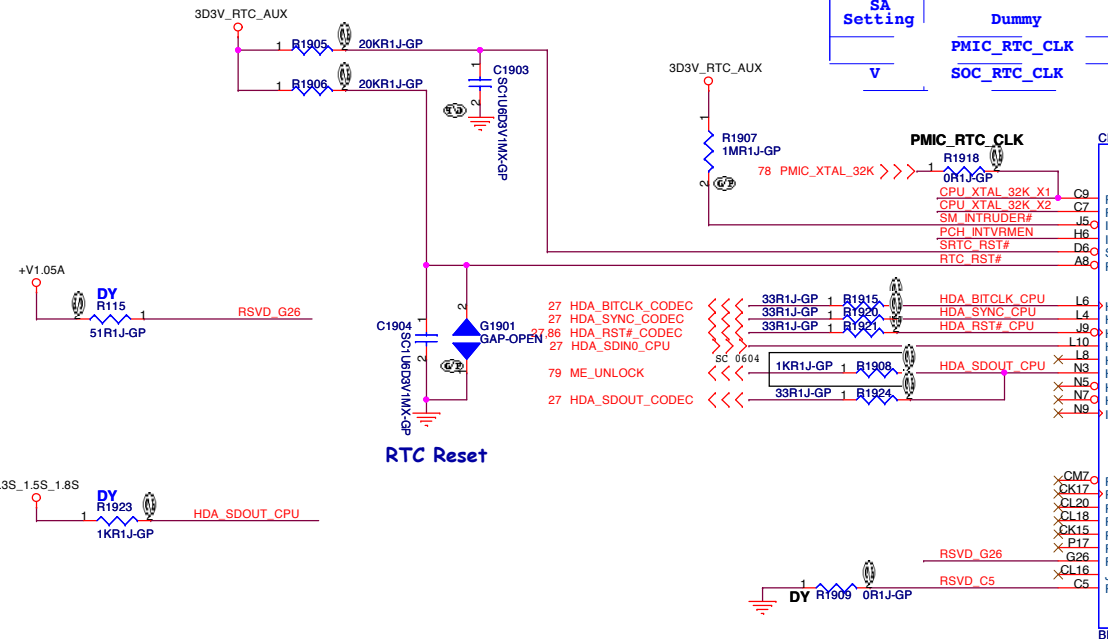
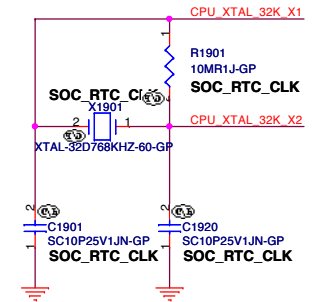
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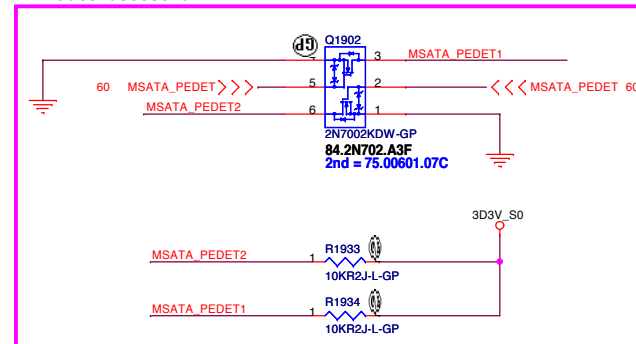
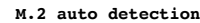
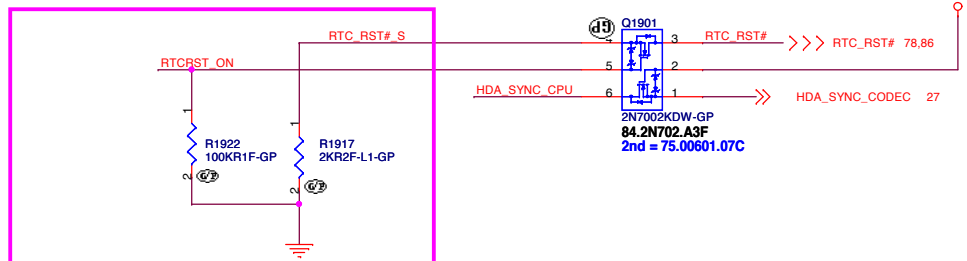
SSID = PCH



INTVRMEN- Integrated SUS
1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs



—Layout Note:



Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

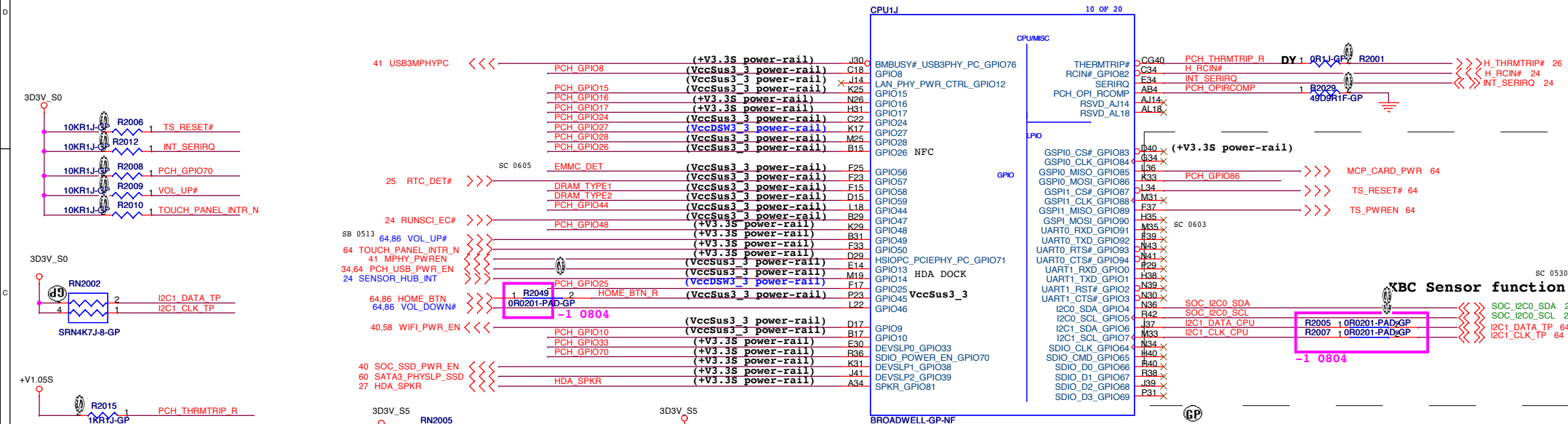
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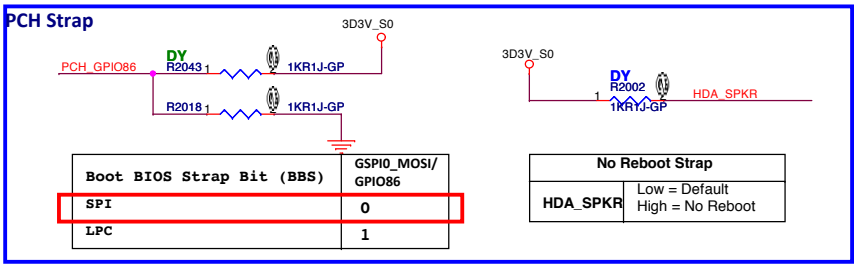
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SSID = PCH



ON-DRAM Strap pin table			
GPIO58	GPIO59	GPIO60	Status (vendor+size)
DRAM_TYPE1	DRAM_TYPE2	DRAM_TYPE3	
0	0	0	Hynix H9CCNNNBPTALBR 4GB
0	0	1	Hynix H9CCNNN8KTALBR 2GB
0	1	0	SAMSUNG K3QF1F10DM 2GB
0	1	1	SAMSUNG K3QF2F20DM 4GB



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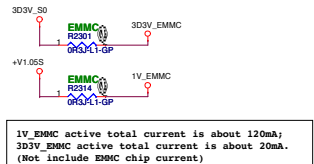
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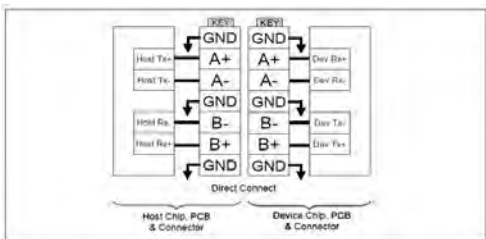
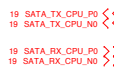
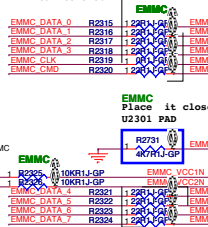
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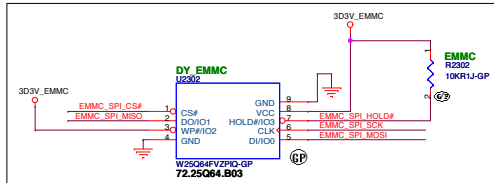


Place these damping resistors near to U2301

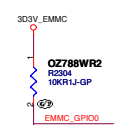


In both cases the connection of the TX differential signal pair on the host side to the RX differential signal pair on the device side. A similar connection of the host RX pair to the device TX pair is also shown.

SPI Flash/EEPROM



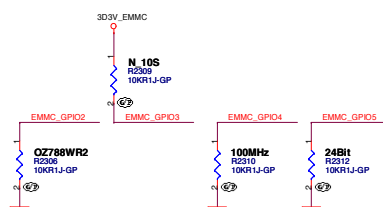
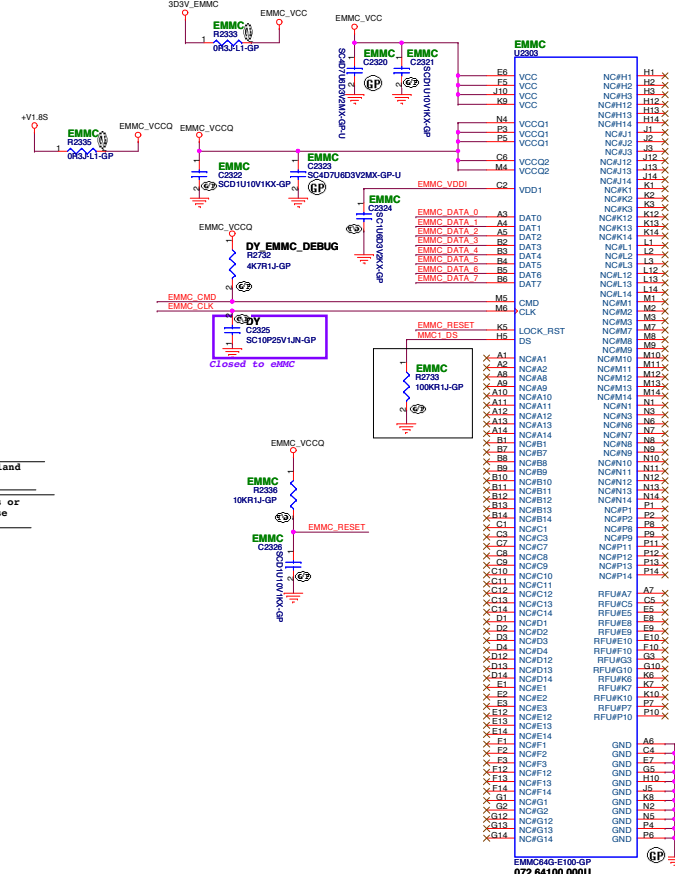
GPIO Setting



When use 0278WR2, pull down GPIO100 to GND;
When use 0278WR2, pull up GPIO100 to P3V3

GPIO1 is LED control signal output as default. If LED is not used, please leave this pin open.

Case	EMMC work mode/ VCCQ (I/O power)	EMMC Spec	Interface Speed	VCCQ	For cost down usage	For EMMC power control usage
1	DDR52 3.3V I/O	eMMC v4.41	104MB/s	3.3V	Solder R3, R4; Don't solder *Q5, **Q3, **R404 and **Q6, **Q4, **R405 control circuit; Don't PET control circuit.	Solder *Q5, **Q3, **R404 and **Q6, **Q4, **R405 PET control circuit; Don't solder R3, R4.
2	DDR52 1.8V I/O	eMMC v4.41	104MB/s	1.8V		
3	HS200 1.8V I/O	eMMC v4.5 eMMC v4.51	200MB/s	1.8V		



GPIO2 can be used as GPIO. And
default is input mode, so please
clump this pin to GND or P3V3
to avoid input floating condition
if customer doesn't use this pin.

GPIO3, GPIO4 and GPIO5 should be
connected to GND or P3V3 according to
customer's usage model.

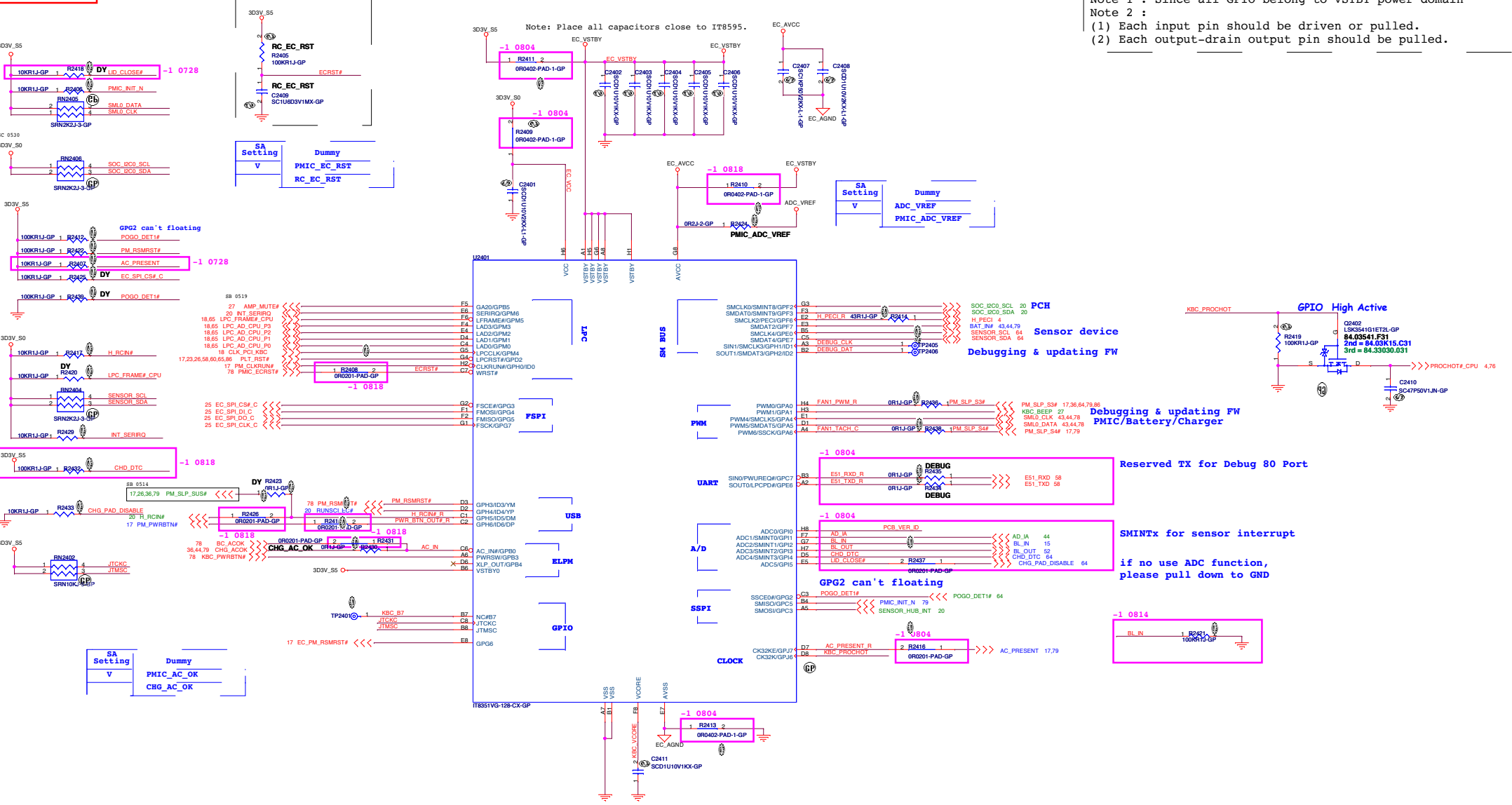
	Pull-down	Pull-up
GPIO0	For 0278WR2, need to pull down GPIO0	For 0278WR2, need to pull up GPIO0
GPIO3	FW will wait init done bit set or 10s time out	FW skip 10s time out
GPIO4	100MHz CPU clock frequency	50MHz CPU clock frequency
GPIO5	SPI 24bit Mode	SPI 16bit Mode

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SSID = KBC

KBC Reset



Note 1 : Since all GPIO belong to VSTBY power domain
Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

PCB VERSION A/D(A13)	R2403		VOLTAGE
	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
SD	100.0K	47.0K	2.24V
SE	100.0K	64.9K	2.0V
-1	100.0K	76.8K	1.87V
-2	100.0K	100.0K	1.65V

SPI ROM Equal length need to less than 500mil

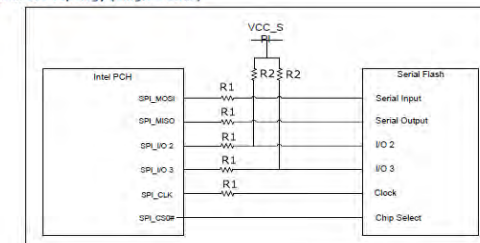


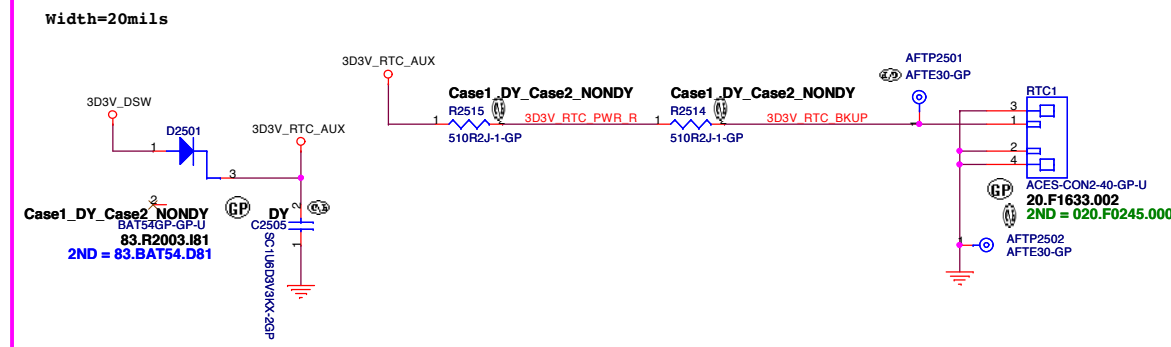
Table 28-2. SPI Flash Device(s) and TPM Routing Guideline (Sheet 2 of 2)

Parameter	Segment	Stackup	Unit	Routing Recommendation
Resistor	R1		ohm	15
	R2		ohm	1k
	R3		ohm	33

Notes:

1. SP#_CLK must be 20 mils spacing from any other high frequency (>1 GHz) signal.
2. Place R1 closer to driver side to effectively dampen the undershoot and overshoot.
3. All TPM branches/connectors (TPM_MISO, TPM_MISO, TPM_CLK, and PCH_CS#) can be left as NC if SP#_TPM is not implemented.

-1 0805



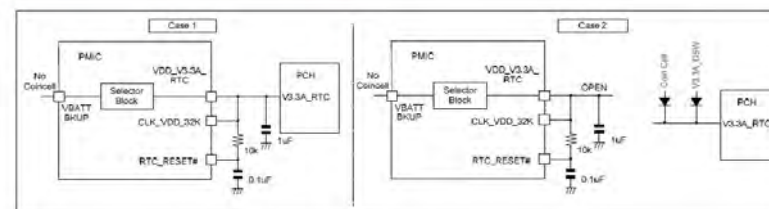
9.4 Coincell battery power reduction

PMIC constantly consumes 15uA (typ.) from VBATTBKUP when the coin cell battery is connected and VDC is under RTC_UVLO VMIN (3.3V/3.6V).
There are ways as the below figure to reduce the power consumption in case that coin cell battery is not used or is not connected to PMIC.

Case 1 Coincell battery is not used

Case 2. Coincell battery is used only for PCH.

Figure 9-3: The connection of coincell power reduction



Coincell battery power reduction (No Coincell)

-1 Setting	LAB Have coincell	Casel	Casel
PR7821	V	V	X
PR7817	V	X	X
PR7905	V	X	X
PR7824	X	V	V
C7812	X	V	V
R2514	X	X	V
R2515	X	X	V
D2501	X	X	V

RTC cell : 023.20006.0001

023.20007.0001

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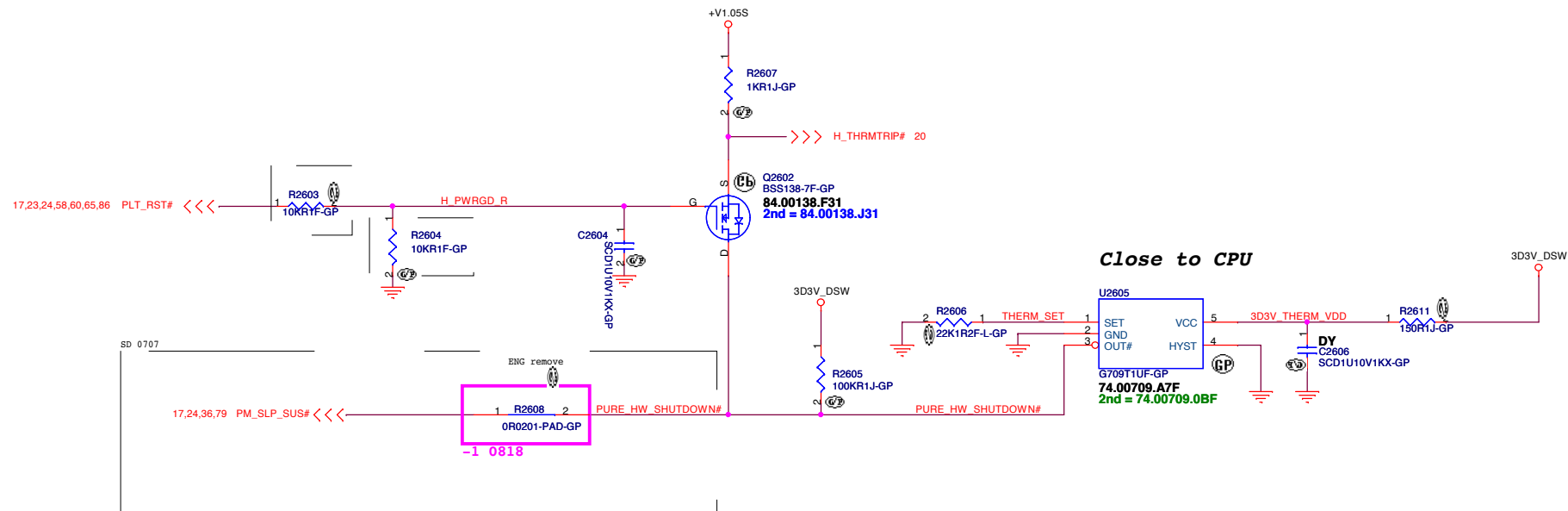
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Flash(KBC+CPU)/RTC			
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Factory Test Function

T8 H/W Shutdown Control circuit

Degree	Rset
95	25.5K
90	22.1K
85	18.7K

Thermal IC Control circuit



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54321

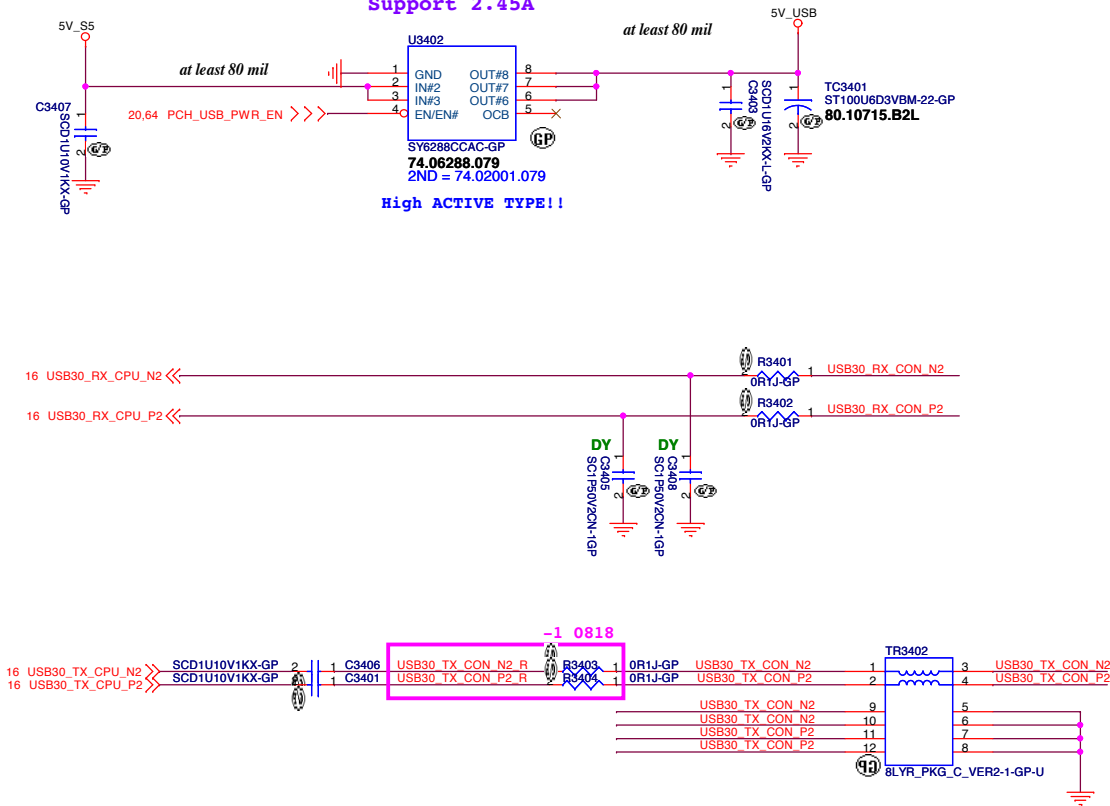
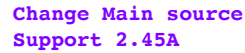
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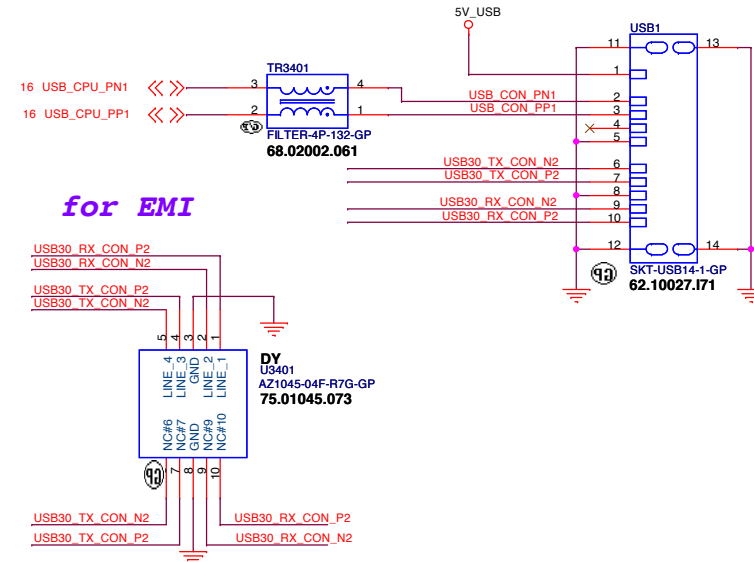
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SSID = USB Port



USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	OTG ID	
5	GND	
6	StdA_SSTX-	SuperSpeed TX
7	StdA_SSTX+	
8	GND	
9	StdA_SSRX-	SuperSpeed RX
10	StdA_SSRX+	



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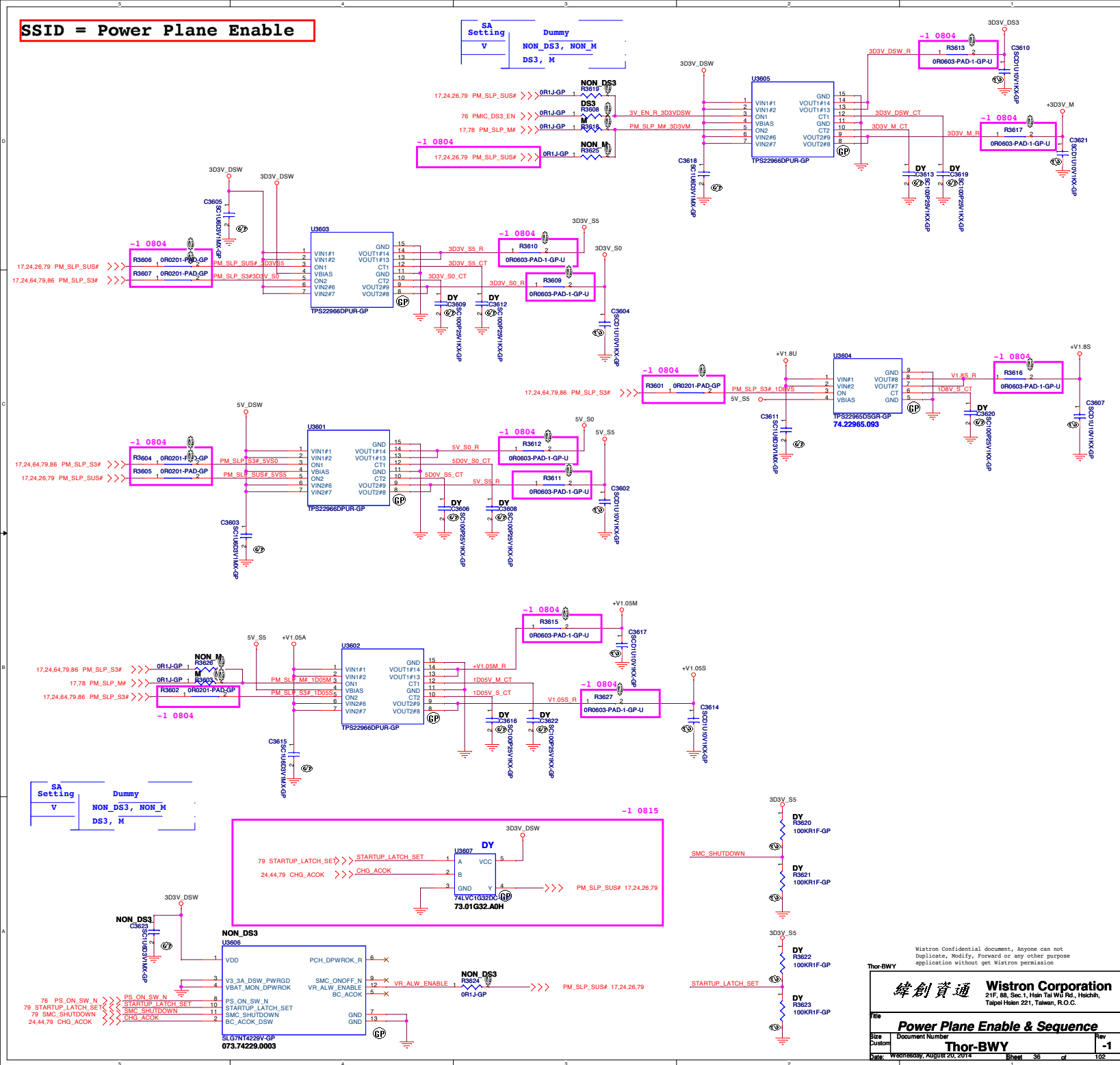
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SSID = Power Plane Enable



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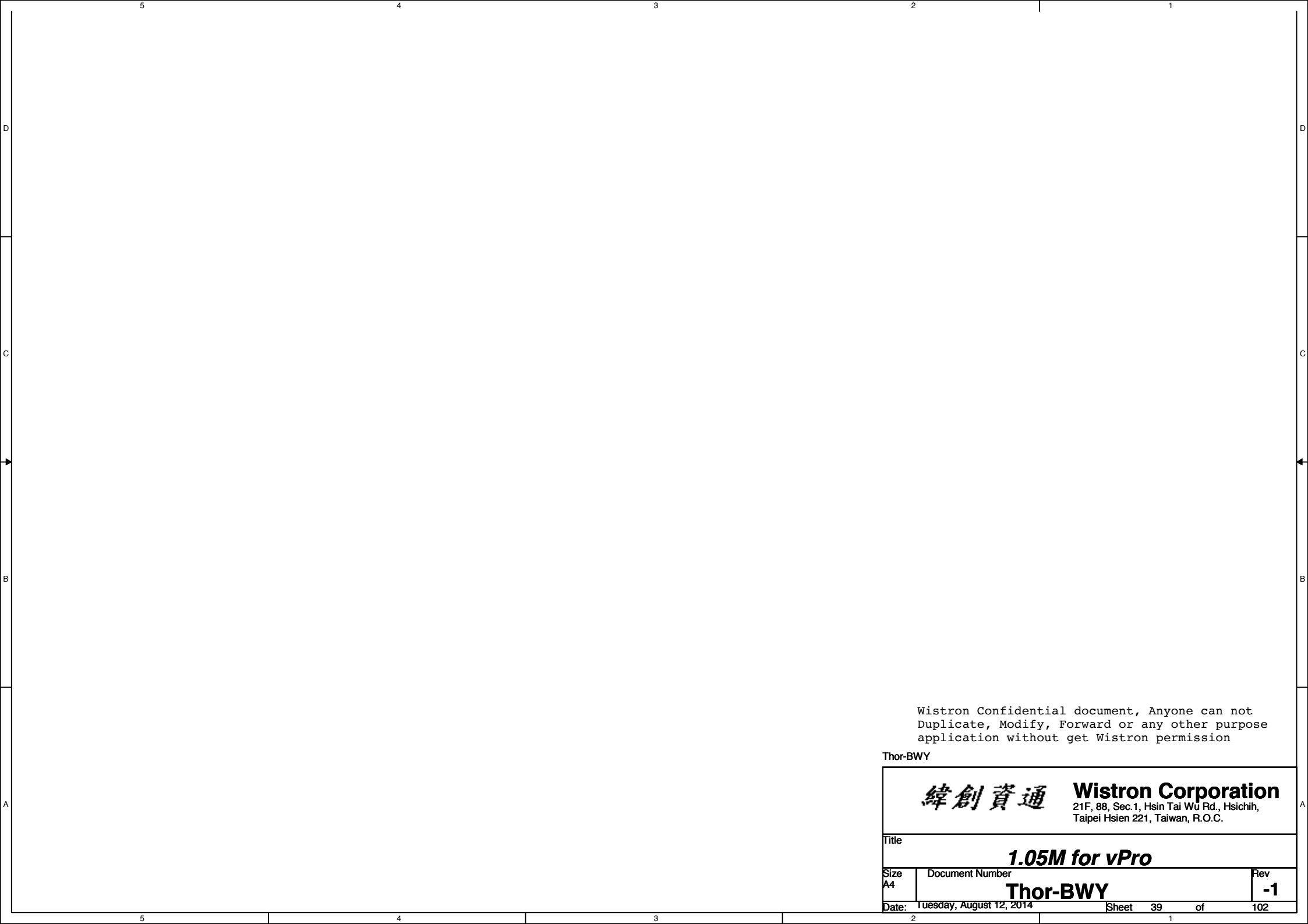
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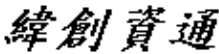
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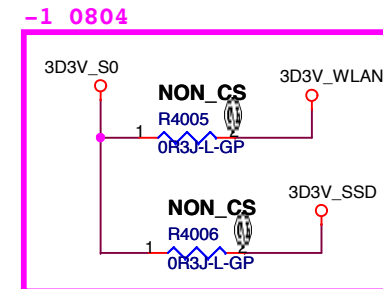
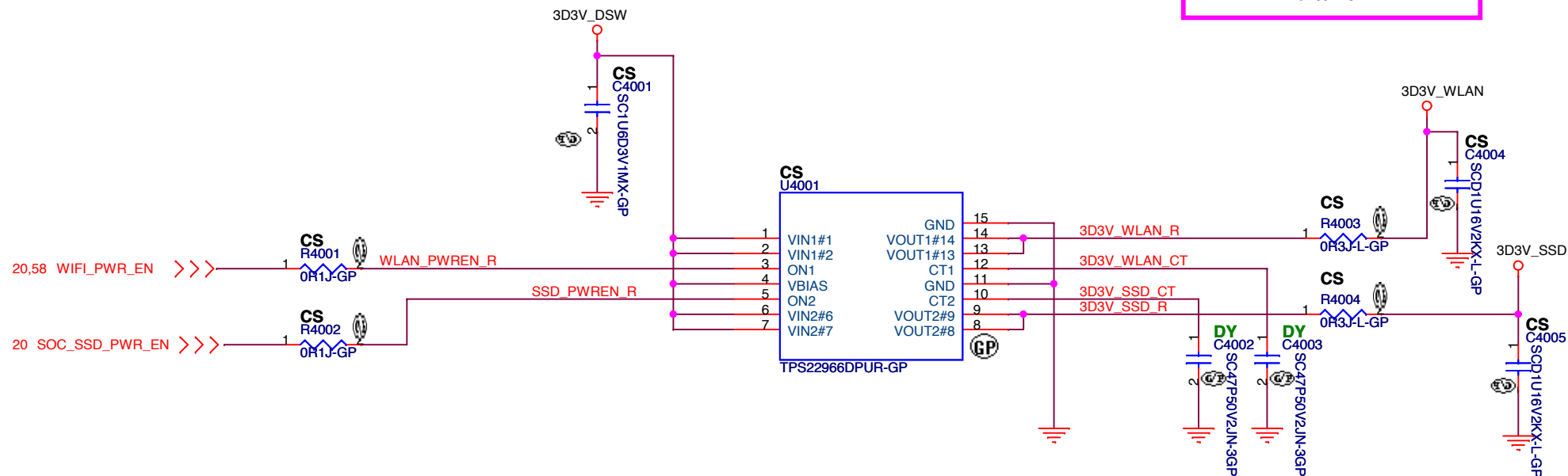
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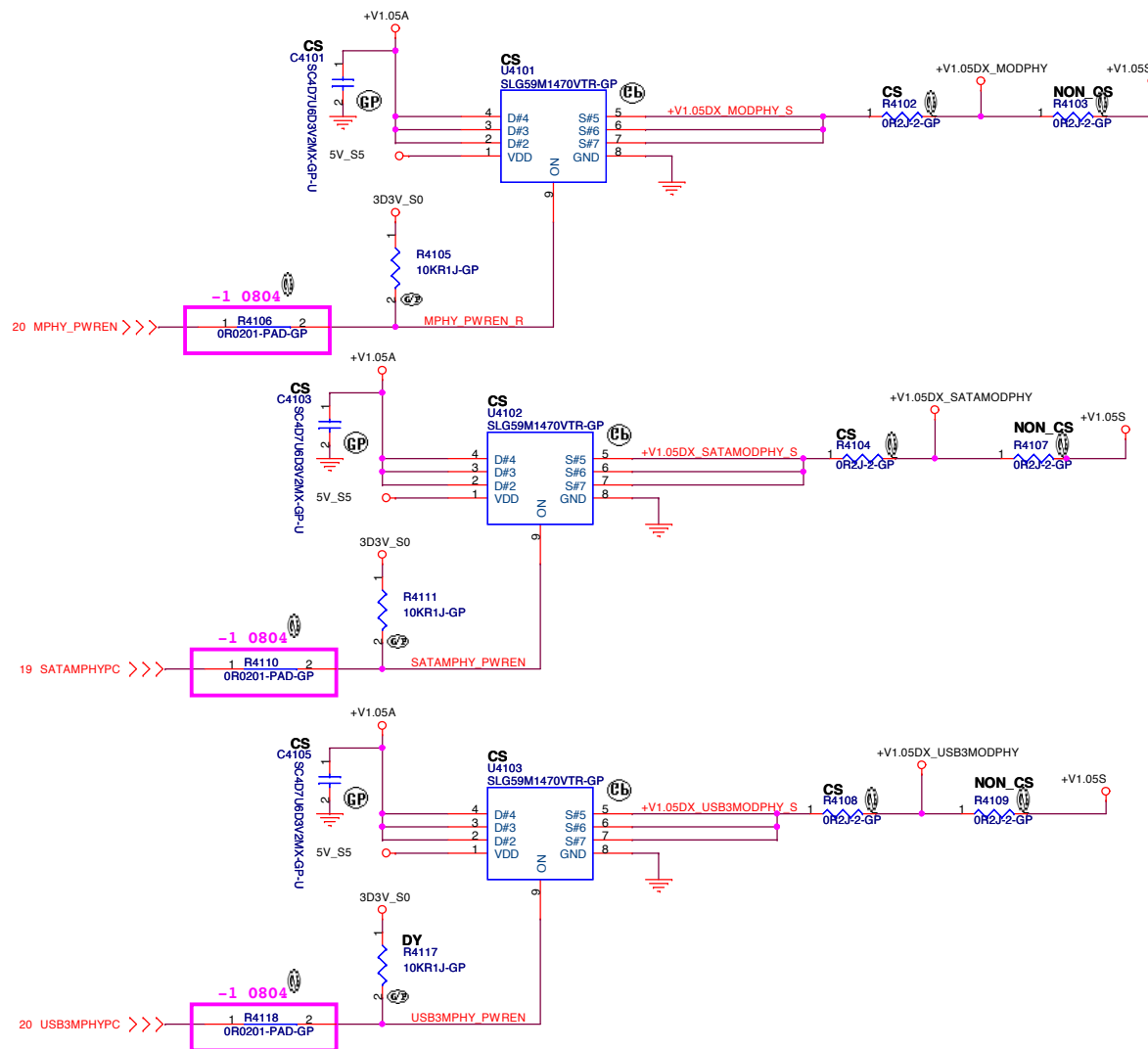
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SSID = Connected Standby



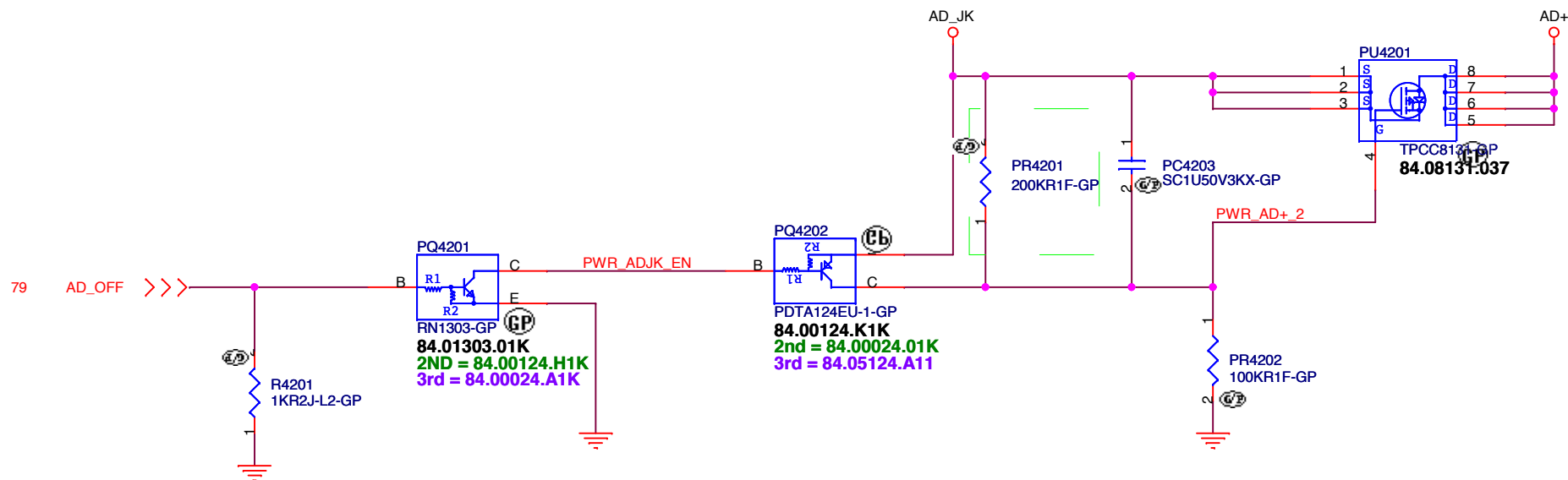
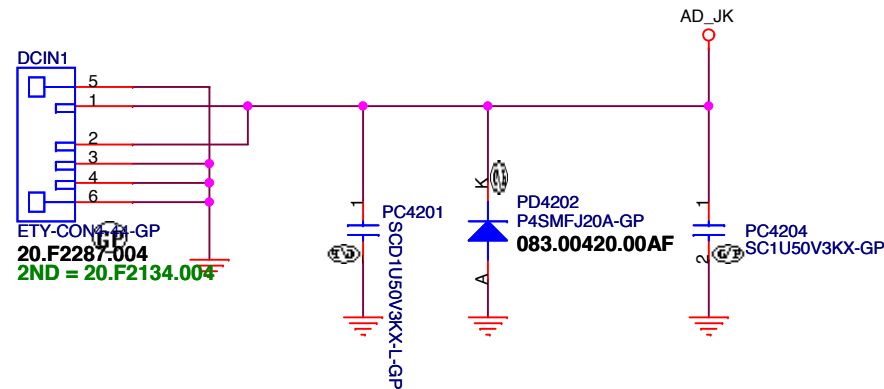
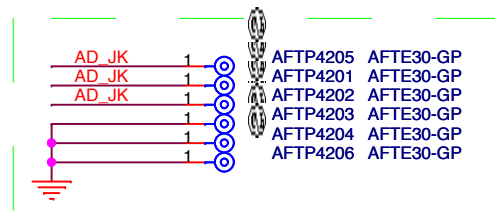
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SSID = PWR.DCIN



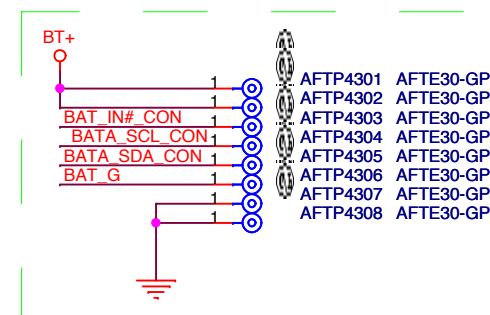
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check battery SPEC pin



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SSID = PWR.Plane.Regulator_5v3p3v

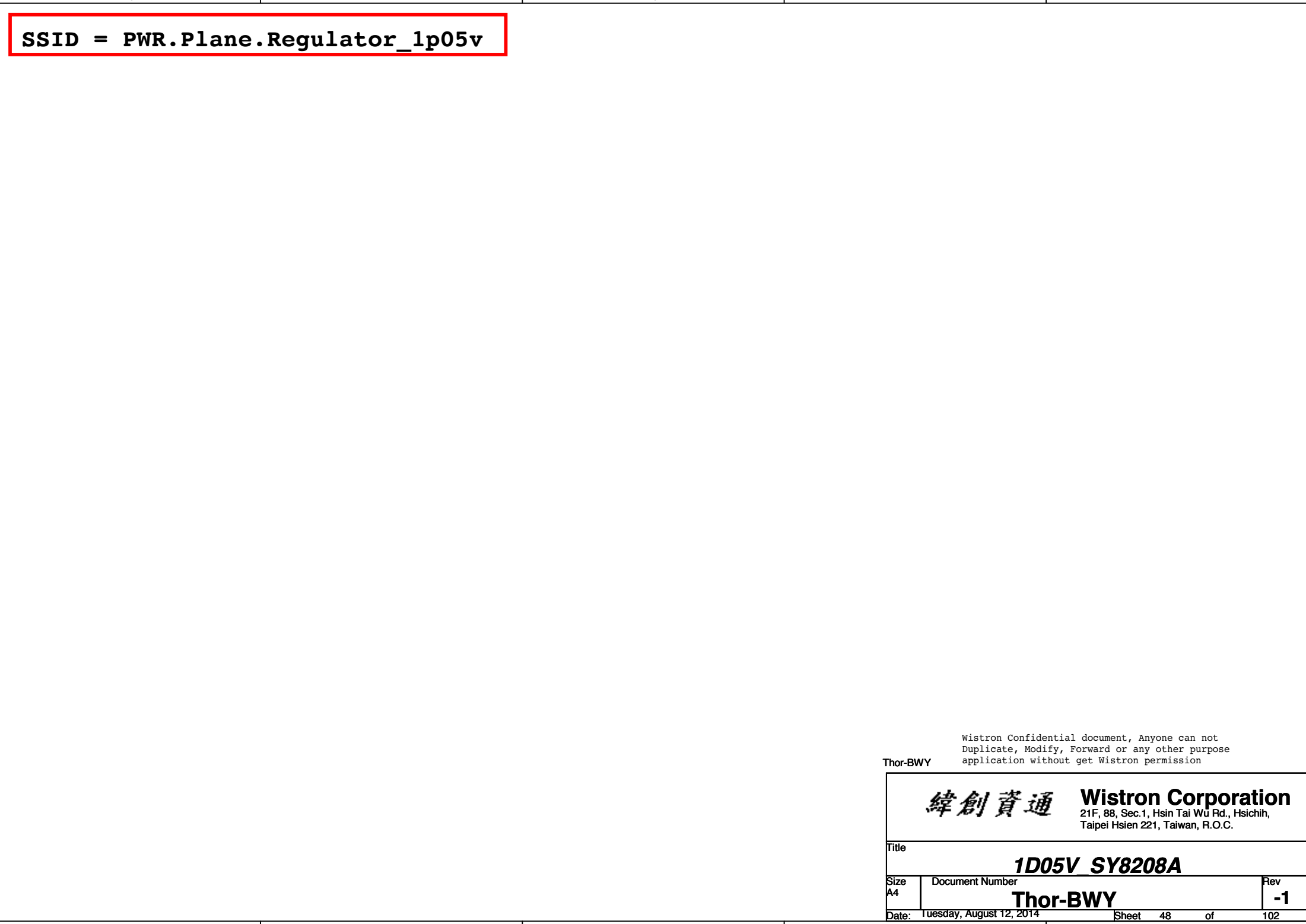
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SYN258B 5V/3D3V			
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SSID = CPU.Regulator

SSID = CPU.Regulator



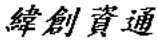
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Title		
1D05V SY8208A		
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SSID = PWR.Plane.Regulator_VTT

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Size A3	Document Number		Rev
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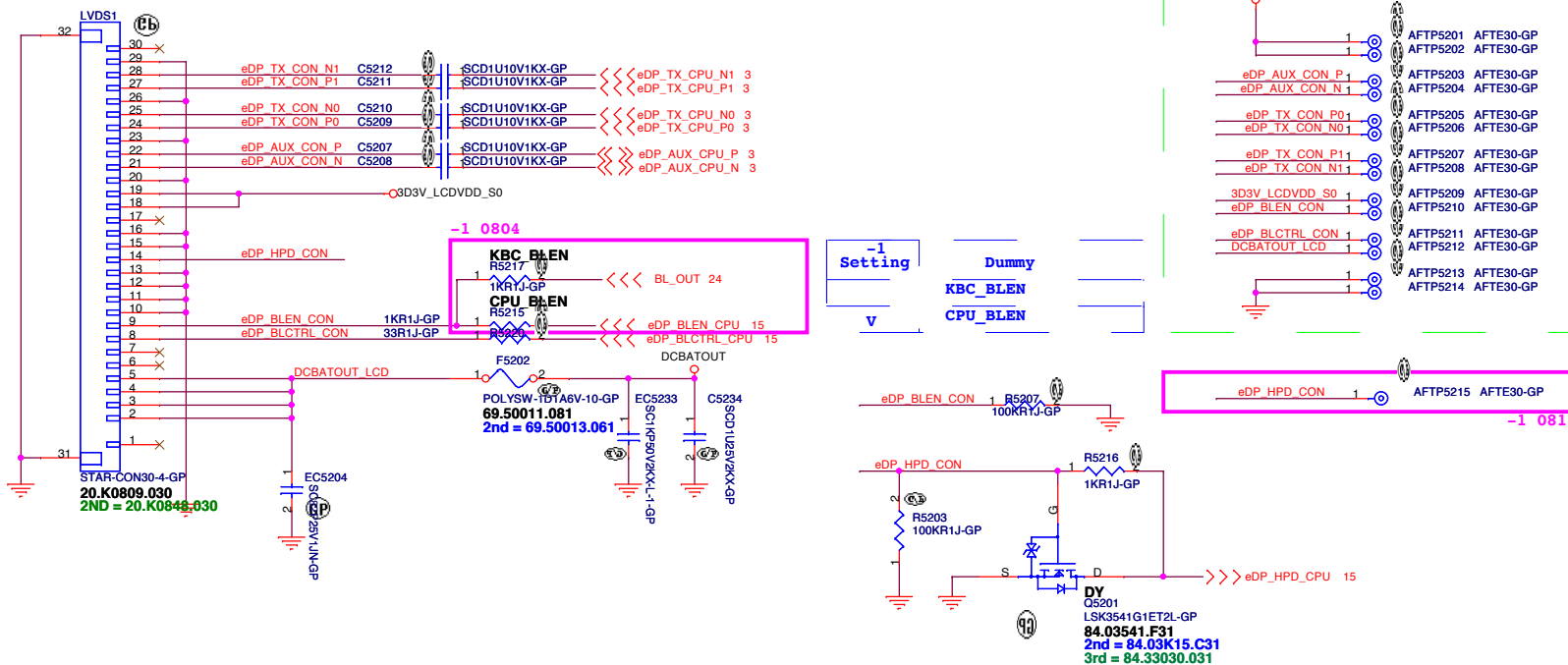
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Size A4	Document Number		Rev
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SSID = 1D5V.Regulator

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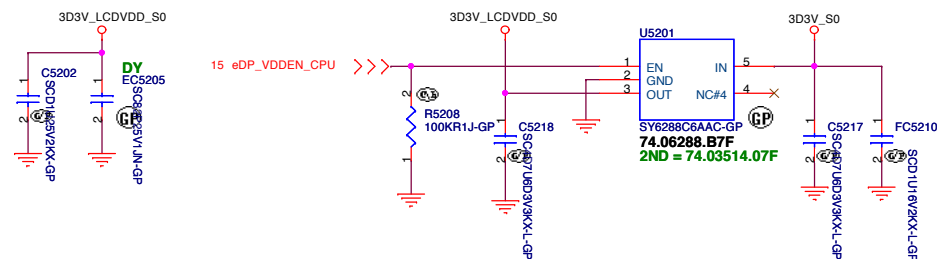
SSID = EDP Connector



Pin	Symbol	Description
1	NC	No Connection (Reserved for LGD)
2	GND	High Speed (Main Link) Ground
3	ML1-	Complement Signal-Lane 1
4	ML1+	True Signal-Main Lane 1
5	GND	High Speed (Main Link) Ground
6	ML0-	Complement Signal-Lane 0
7	ML0+	True Signal-Main Lane 0
8	GND	High Speed (Main Link) Ground
9	AUX+	True Signal-Auxiliary Channel
10	AUX-	Complement Signal-Auxiliary Channel
11	GND	High Speed (Main Link) Ground
12	VCC	VCC for Module (3.3V)
13	VCC	VCC for Module (3.3V)
14	NC	No Connection (Reserved for LGD)
15	GND	LCM Ground (Logic Ground)
16	GND	LCM Ground (Logic Ground)
17	HPD	HPD signal pin
18	GND	LCM Ground (LED Backlight Ground)
19	GND	LCM Ground (LED Backlight Ground)
20	GND	LCM Ground (LED Backlight Ground)
21	GND	LCM Ground (LED Backlight Ground)
22	LED_EN	LED Backlight On/Off
23	PWM	System PWM Signal input for dimming
24	NC	No Connection (Reserved for LGD)
25	NC	No Connection (Reserved for LGD)
26	VLED	LED Backlight Power 5V-21V
27	VLED	LED Backlight Power 5V-21V
28	VLED	LED Backlight Power 5V-21V
29	VLED	LED Backlight Power 5V-21V
30	NC	No Connection (Reserved for LGD)

LP125WF2

Near EDP1 CONN



EDP POWER CIRCUIT

Layout 40 mil

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Title

eDP/Inverter Connector

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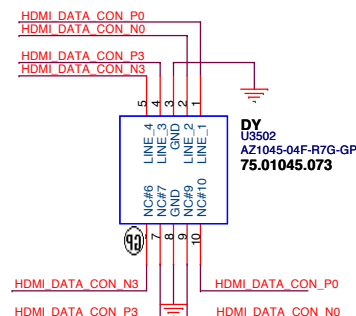
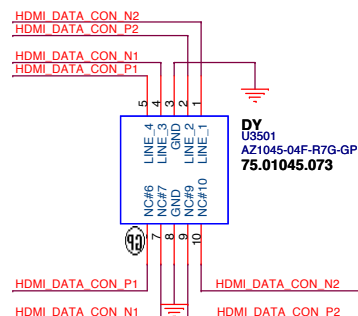
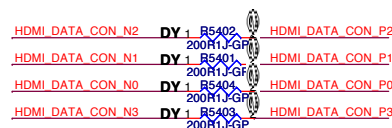
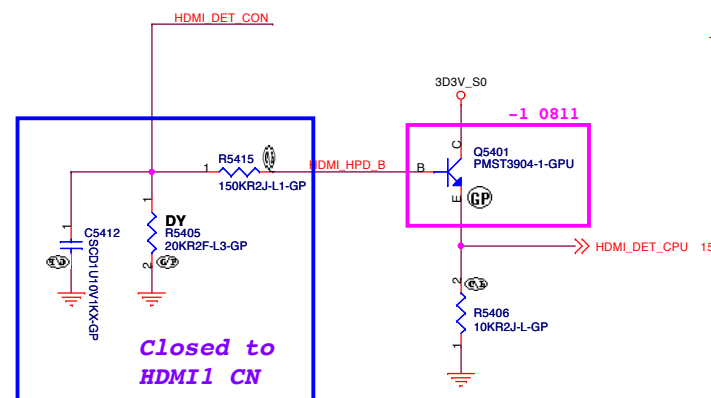
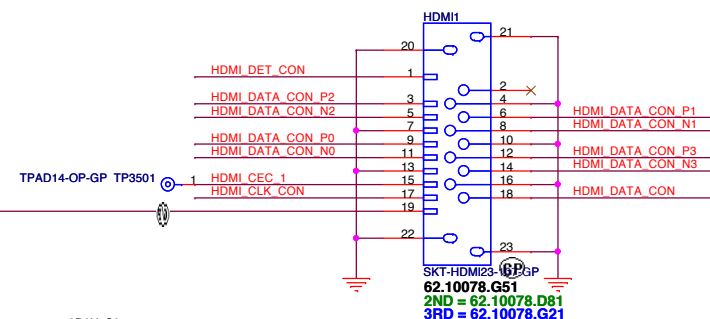
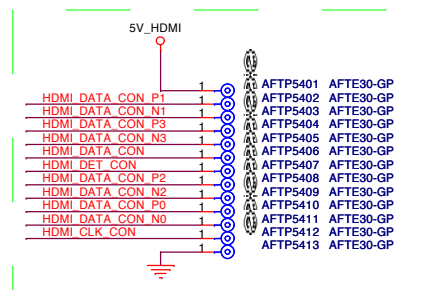
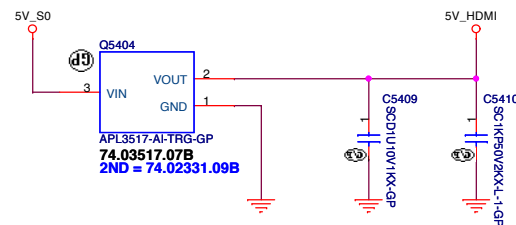
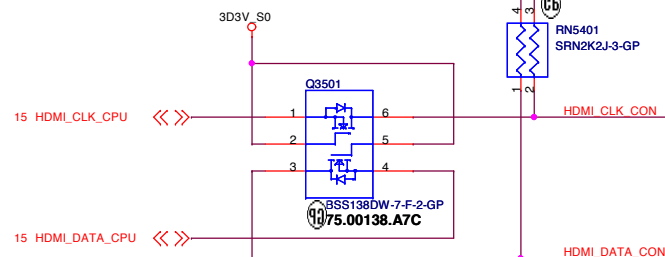
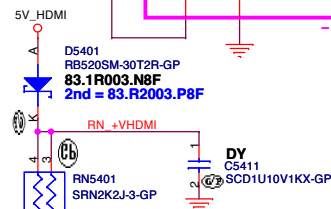
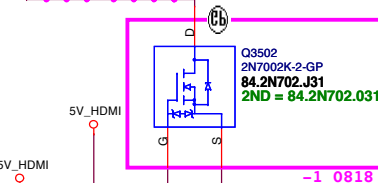
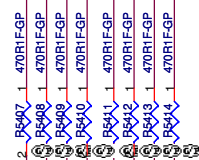
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uHDMI CONN



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Title	HDMI Level Shifter/Conn
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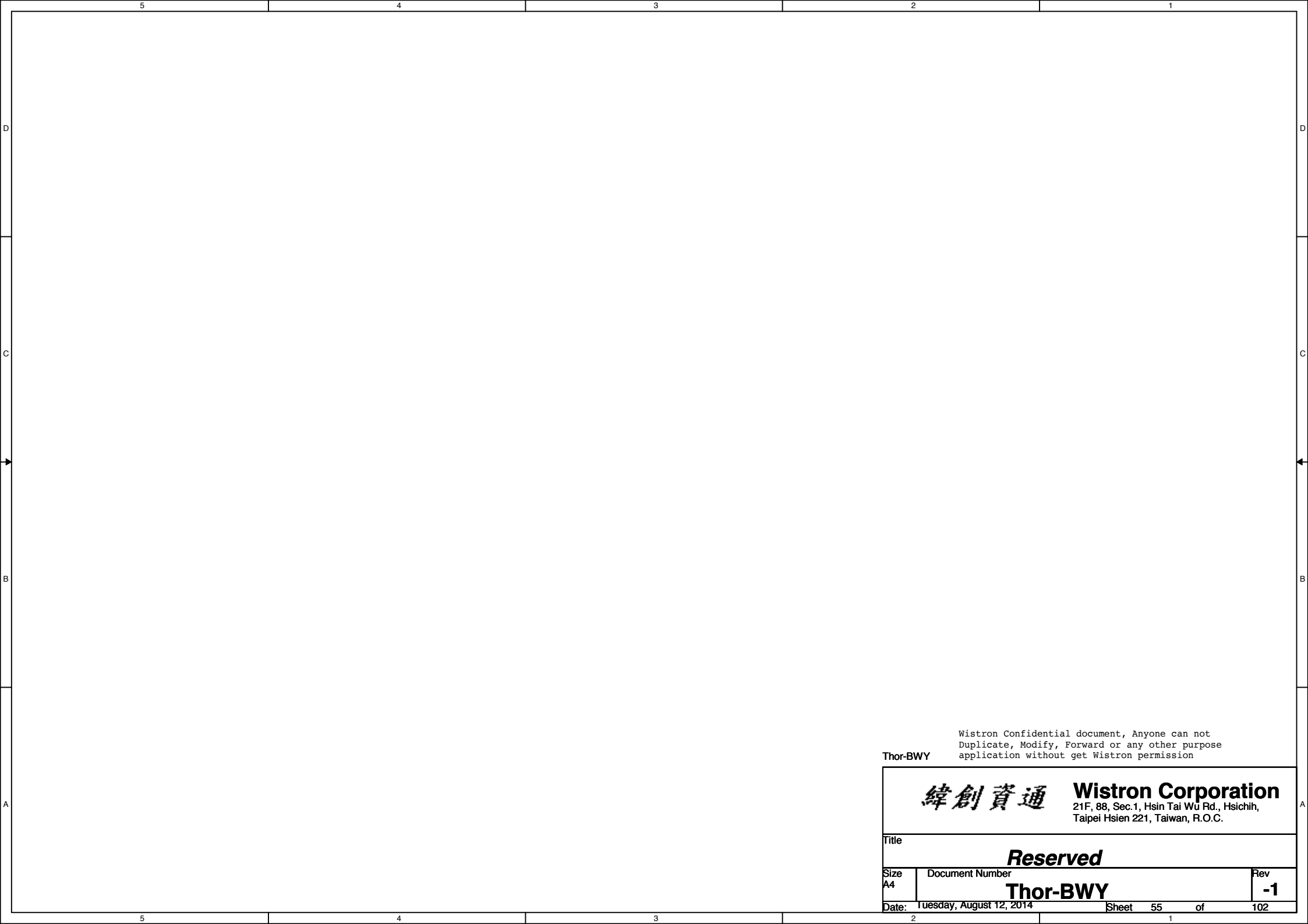
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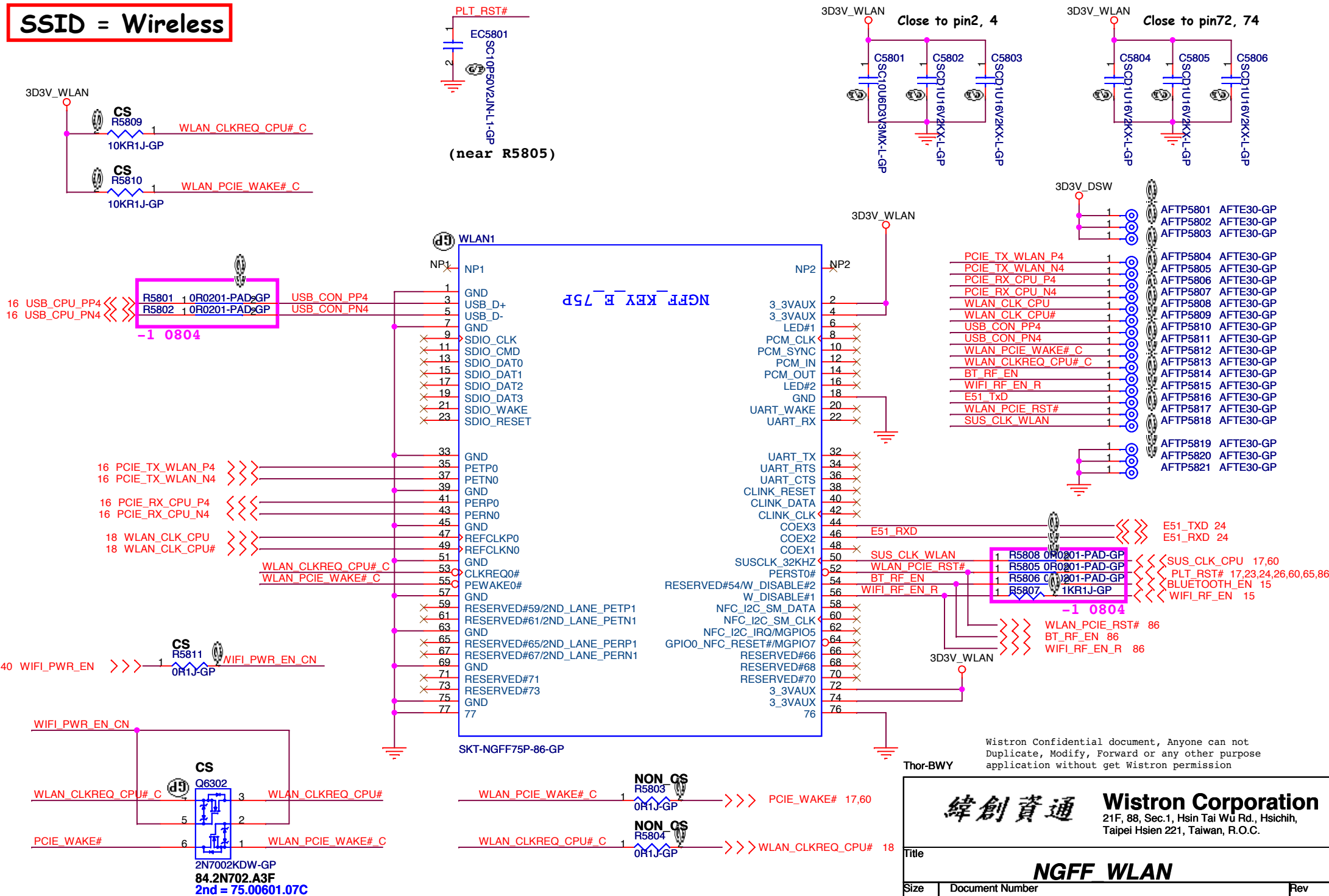
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Date: Tuesday, August 12, 2014

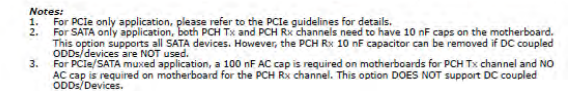
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SSID = Wireless

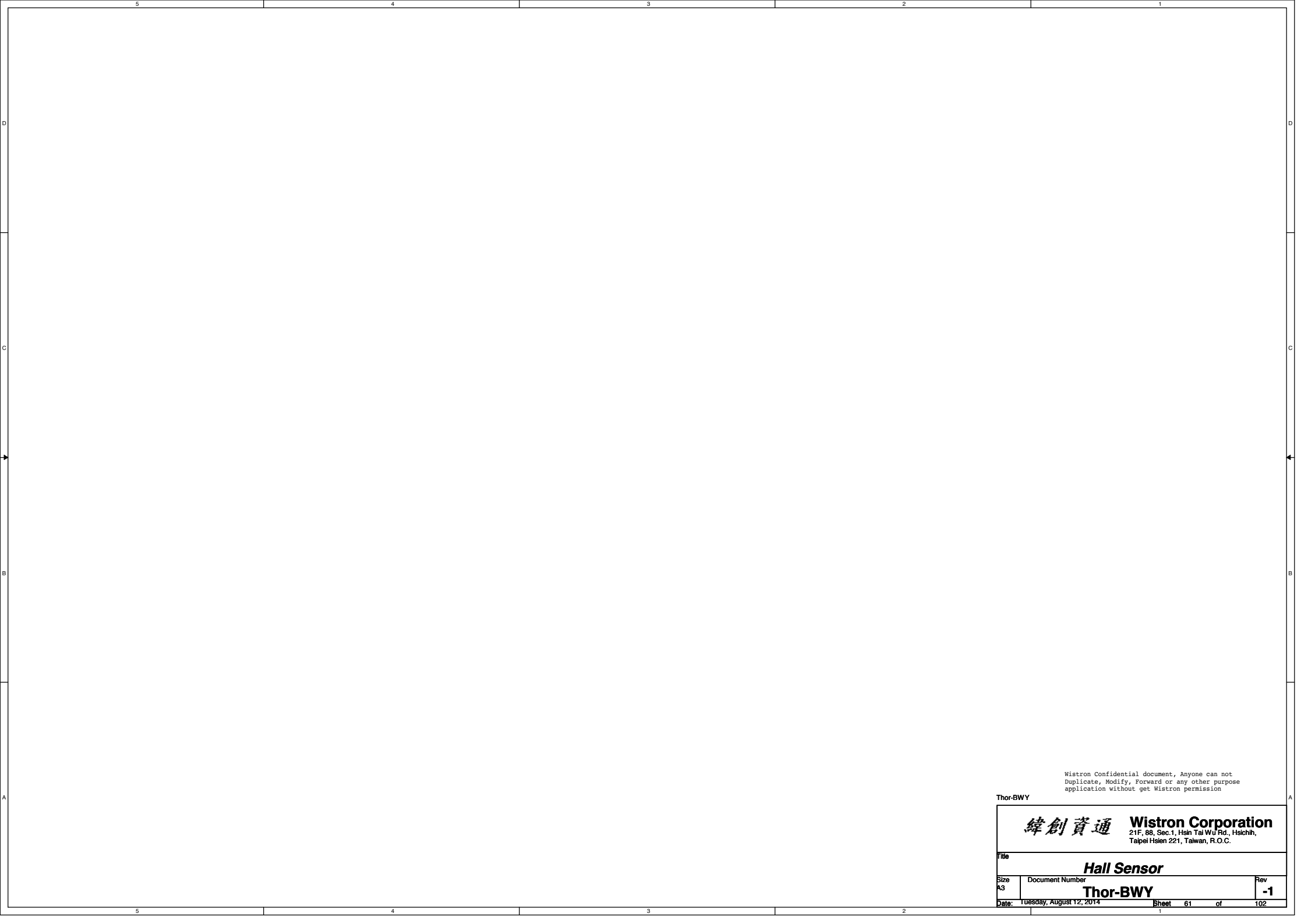


SSID = Wireless

NGFF Conn(SSD)



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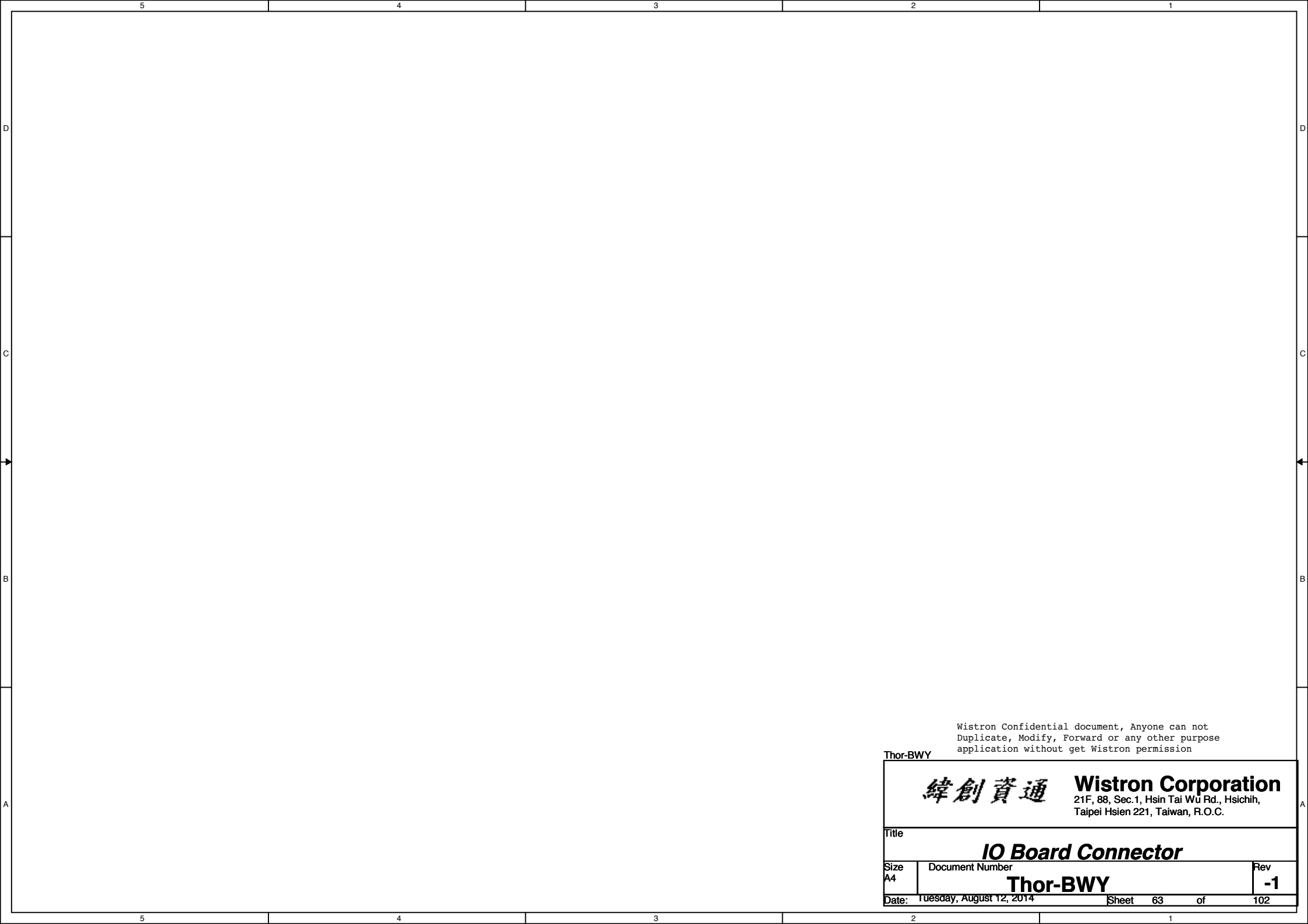
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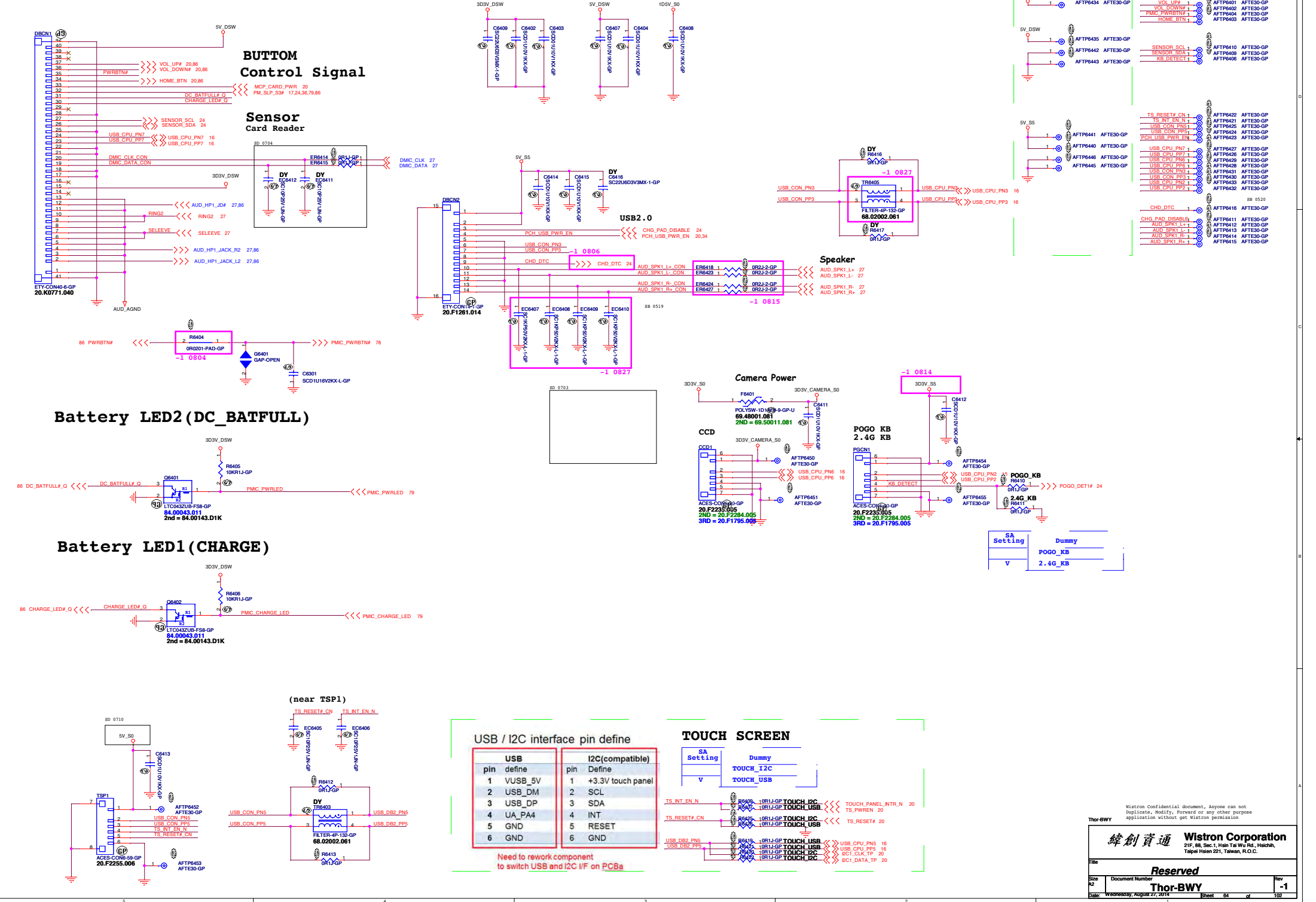


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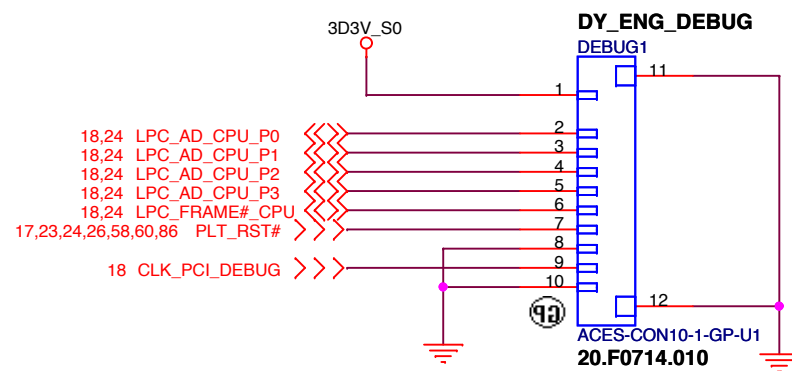
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10 Board Conn.



12 PIN LPC DEBUG CONN.



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Debug connector

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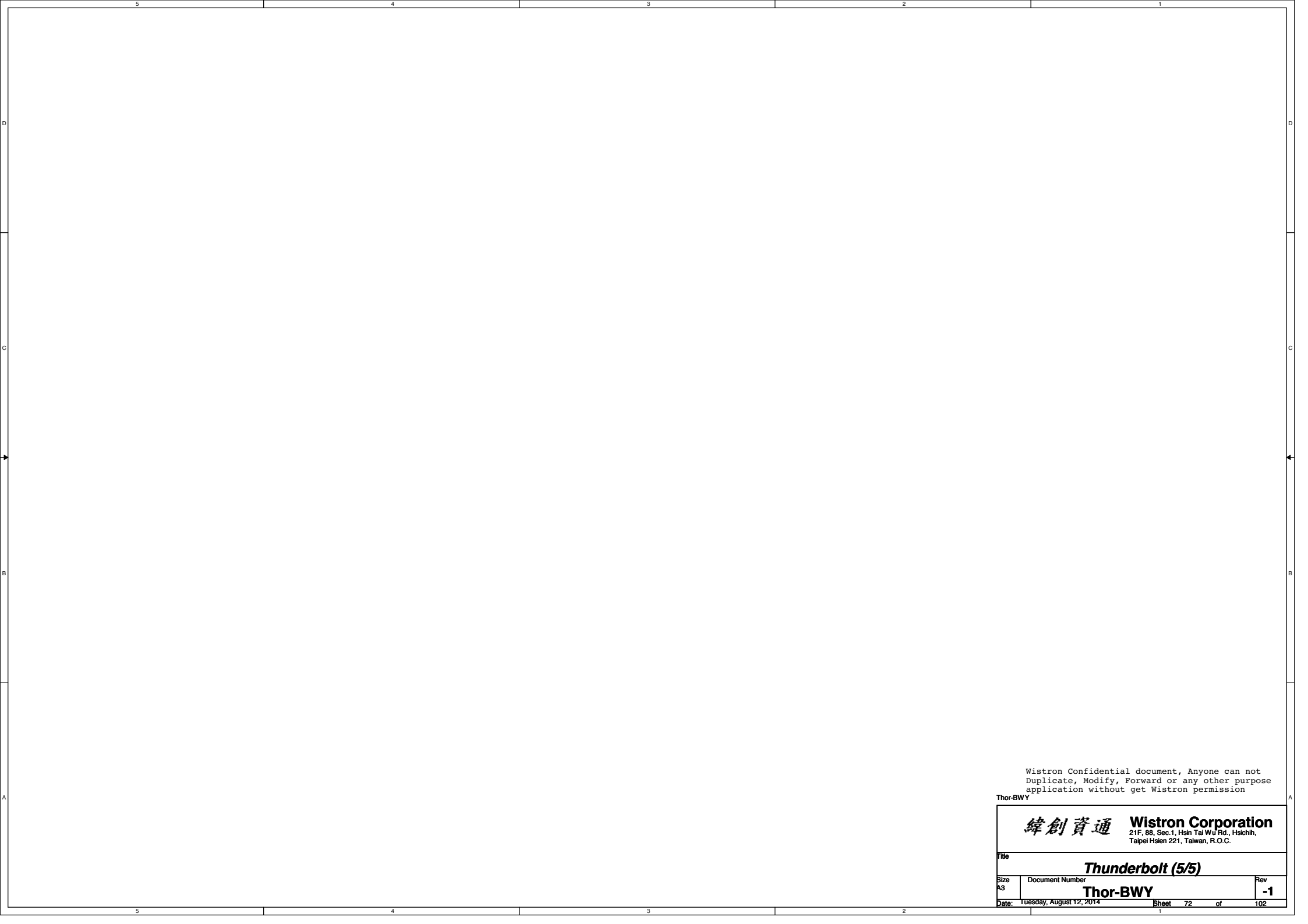
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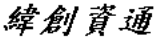
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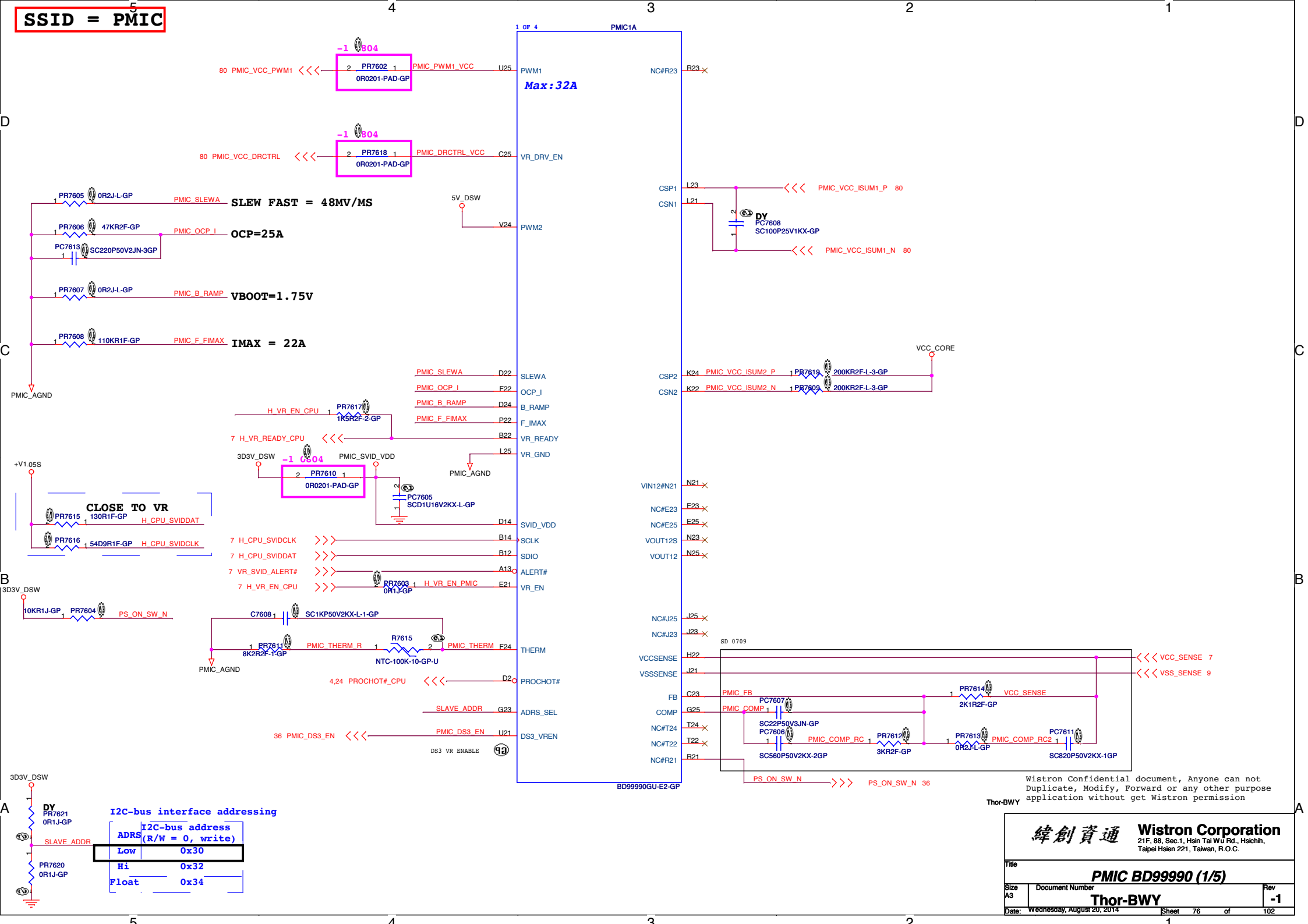
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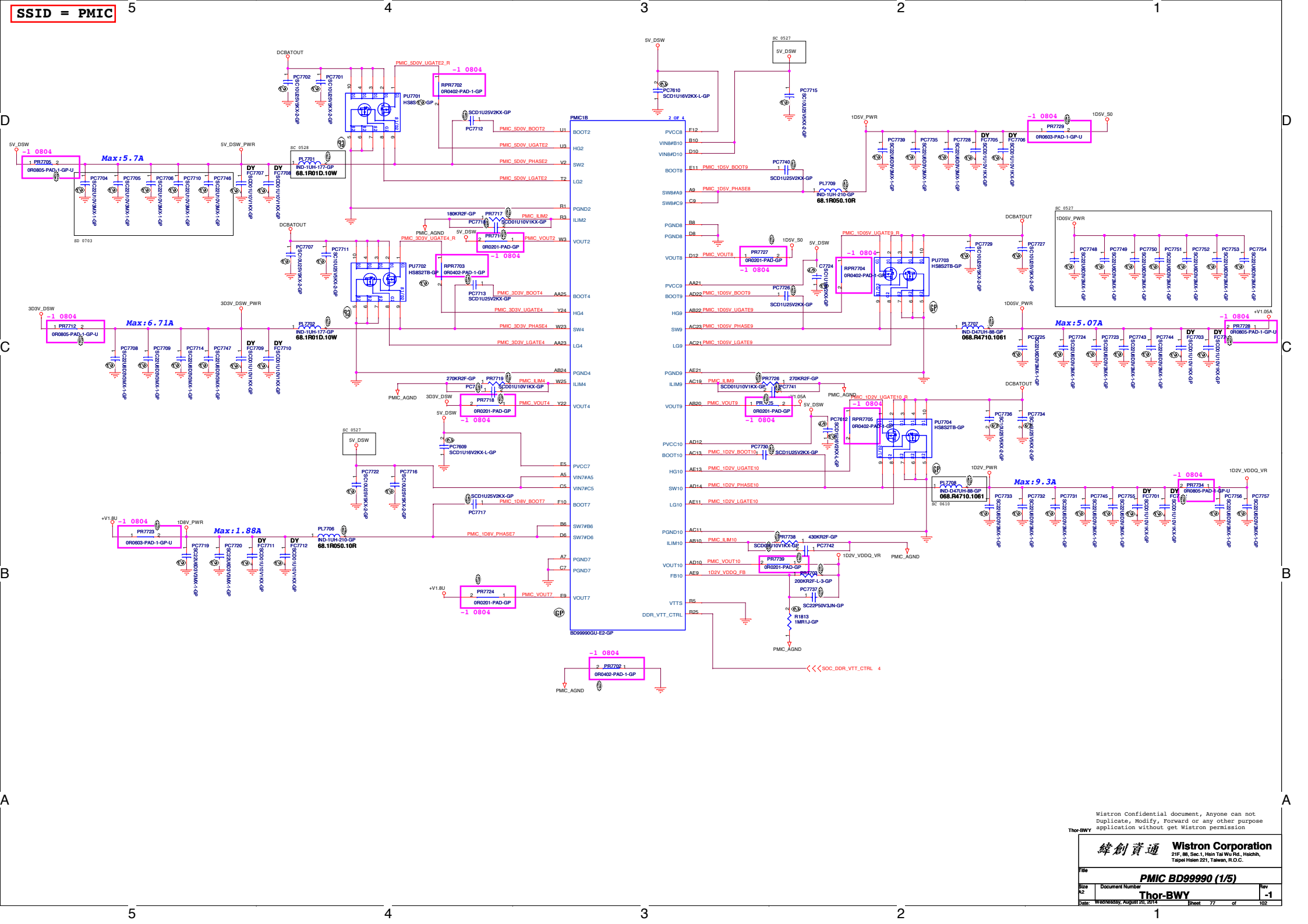
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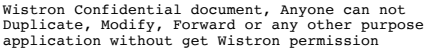
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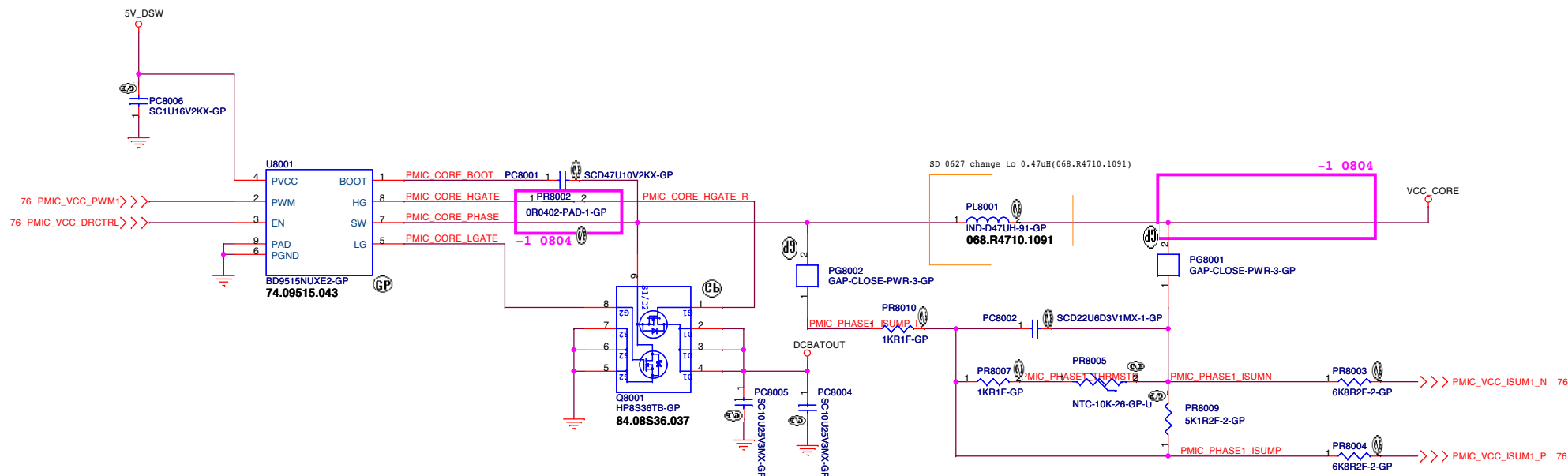
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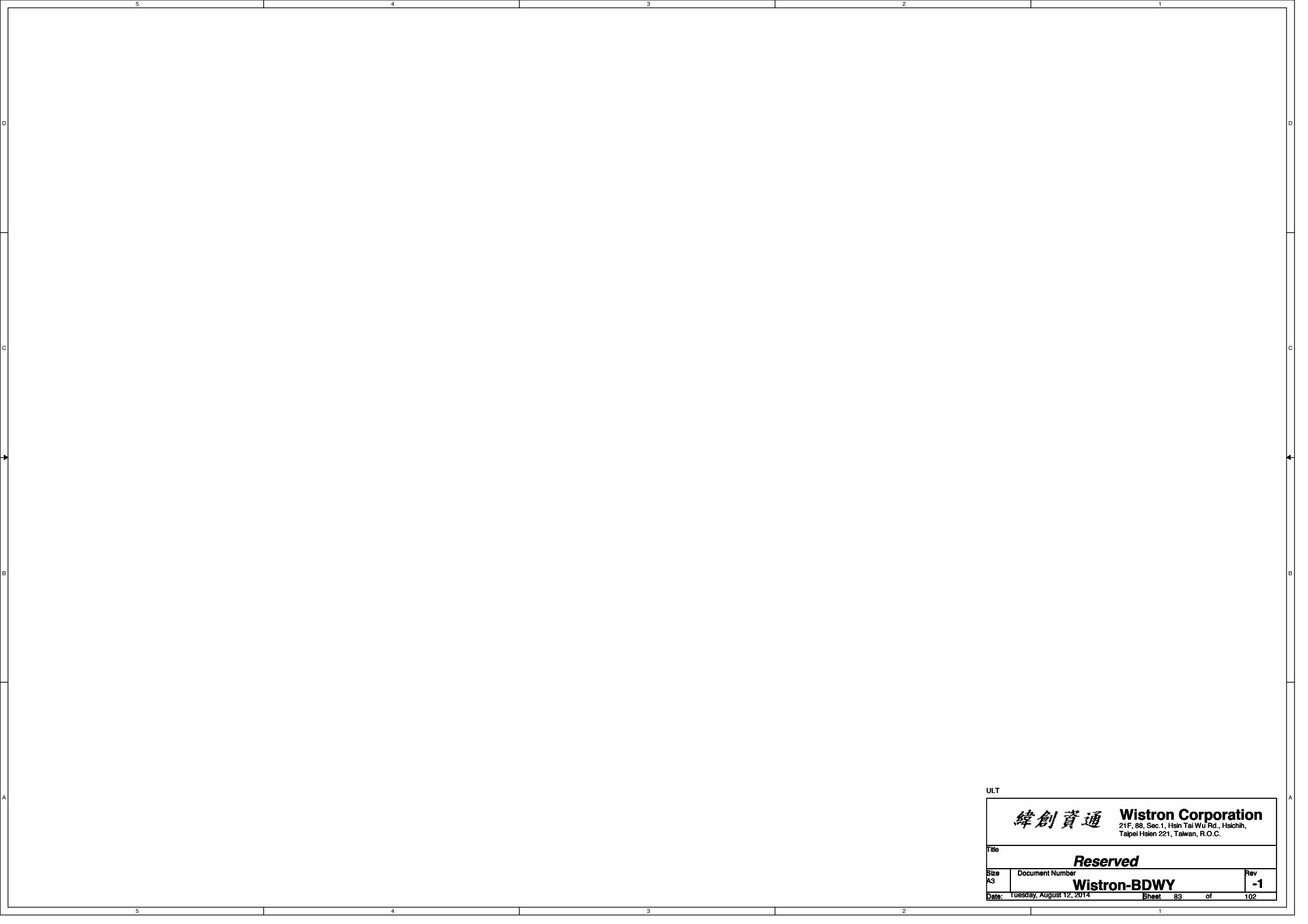
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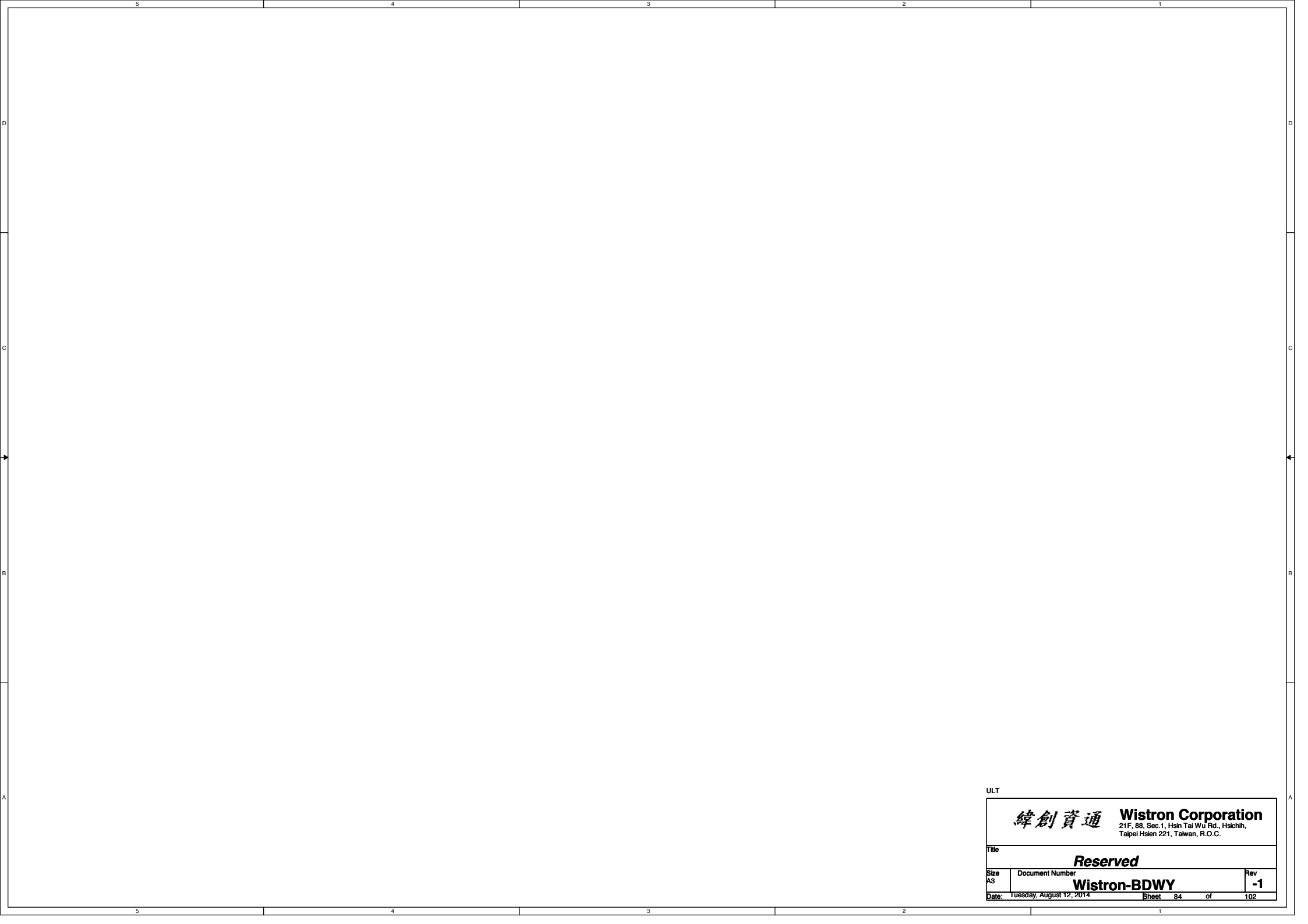
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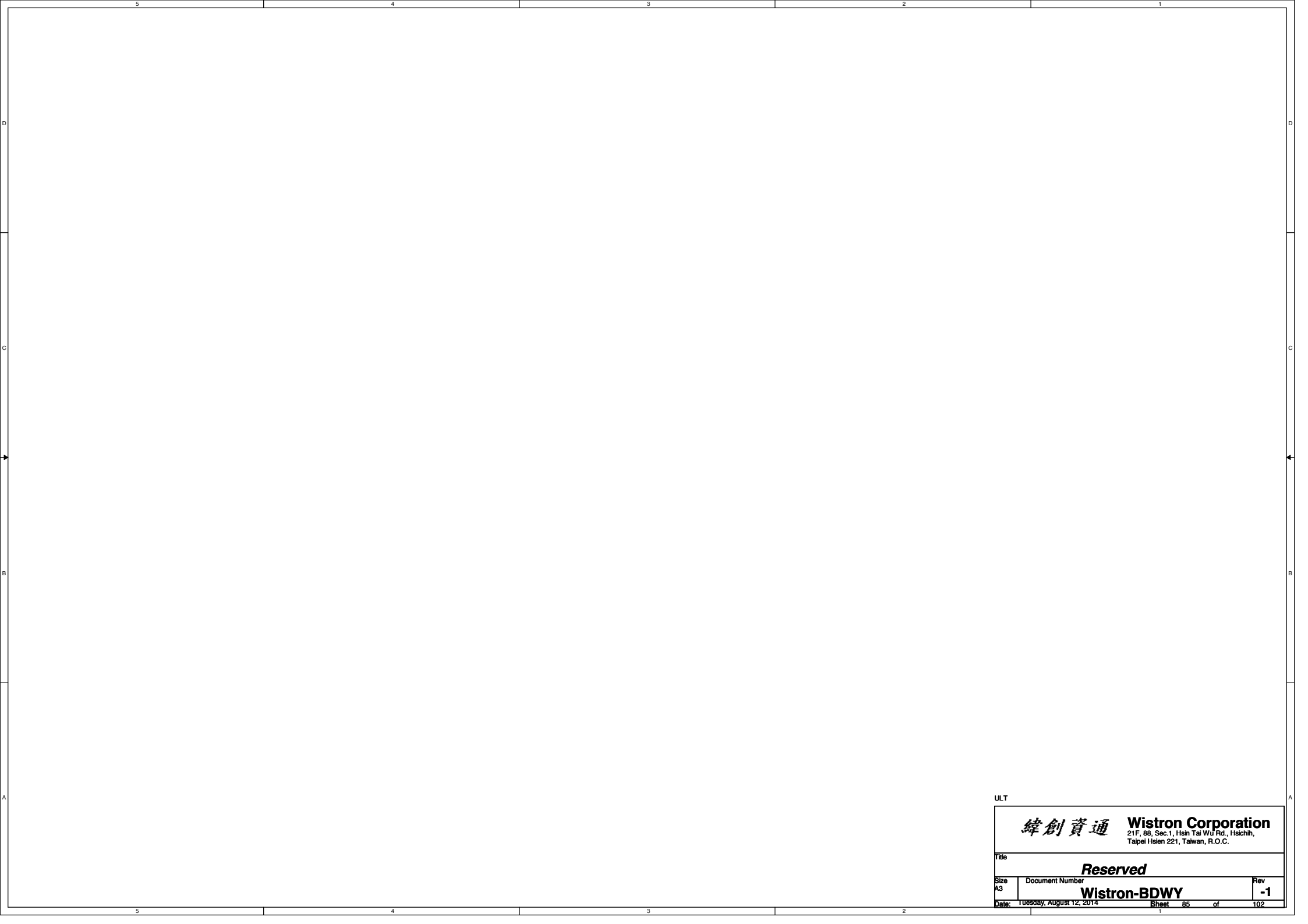
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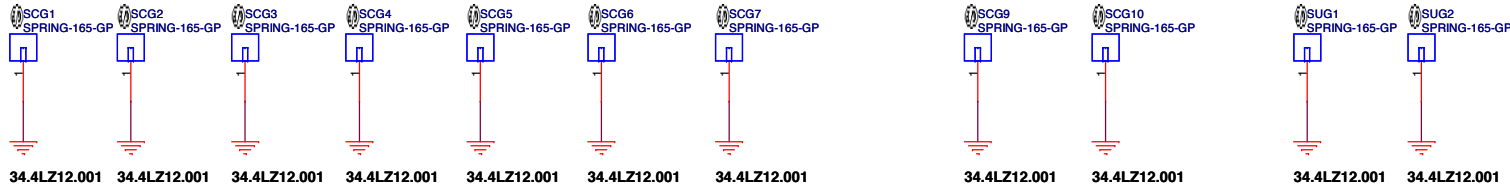
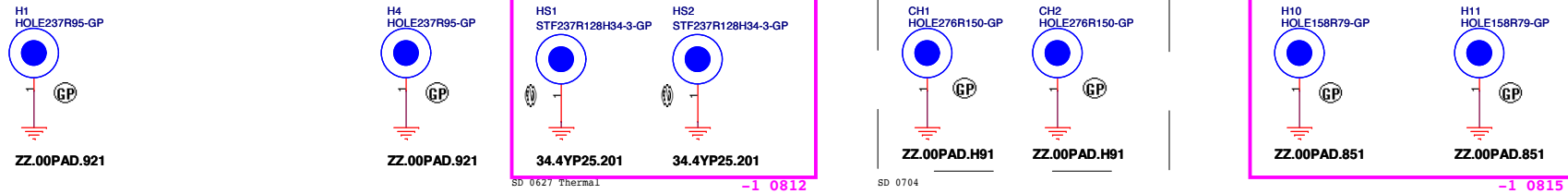
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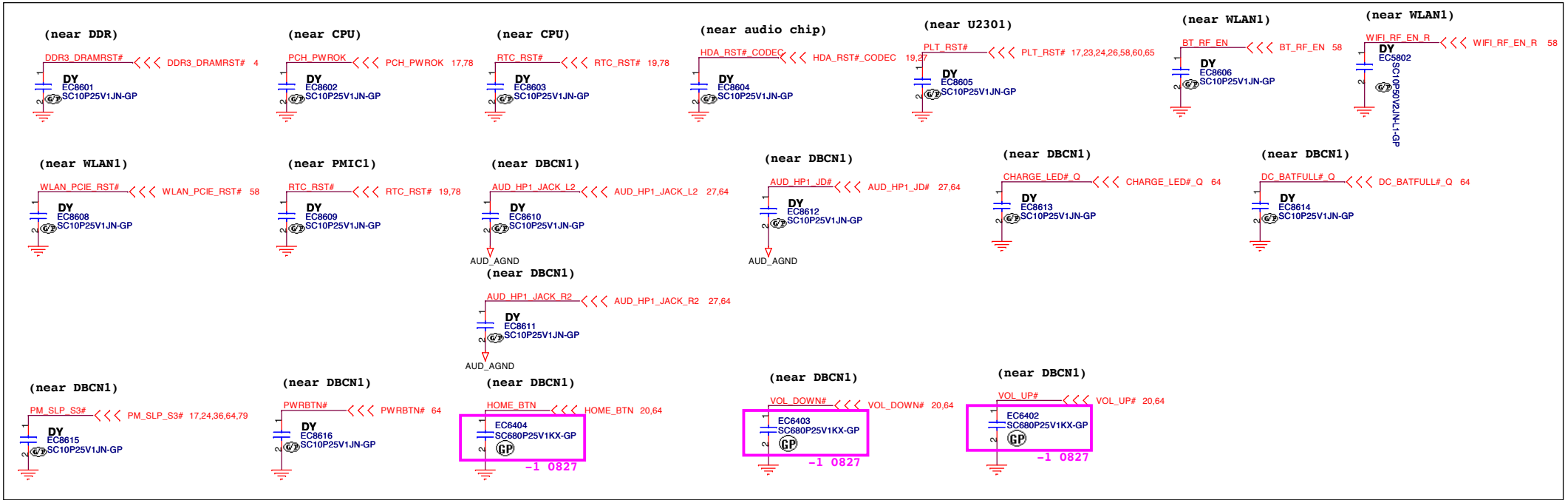
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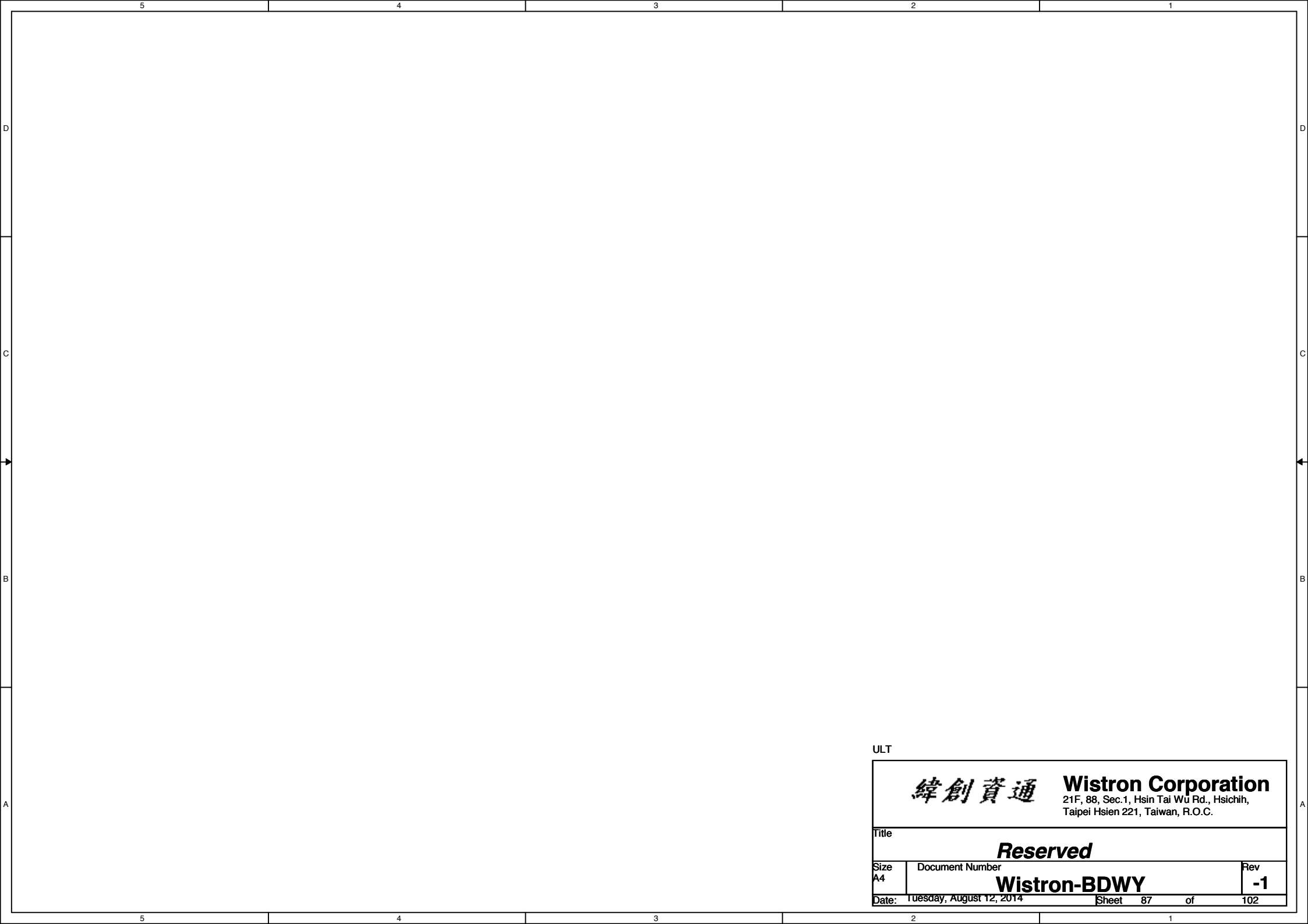
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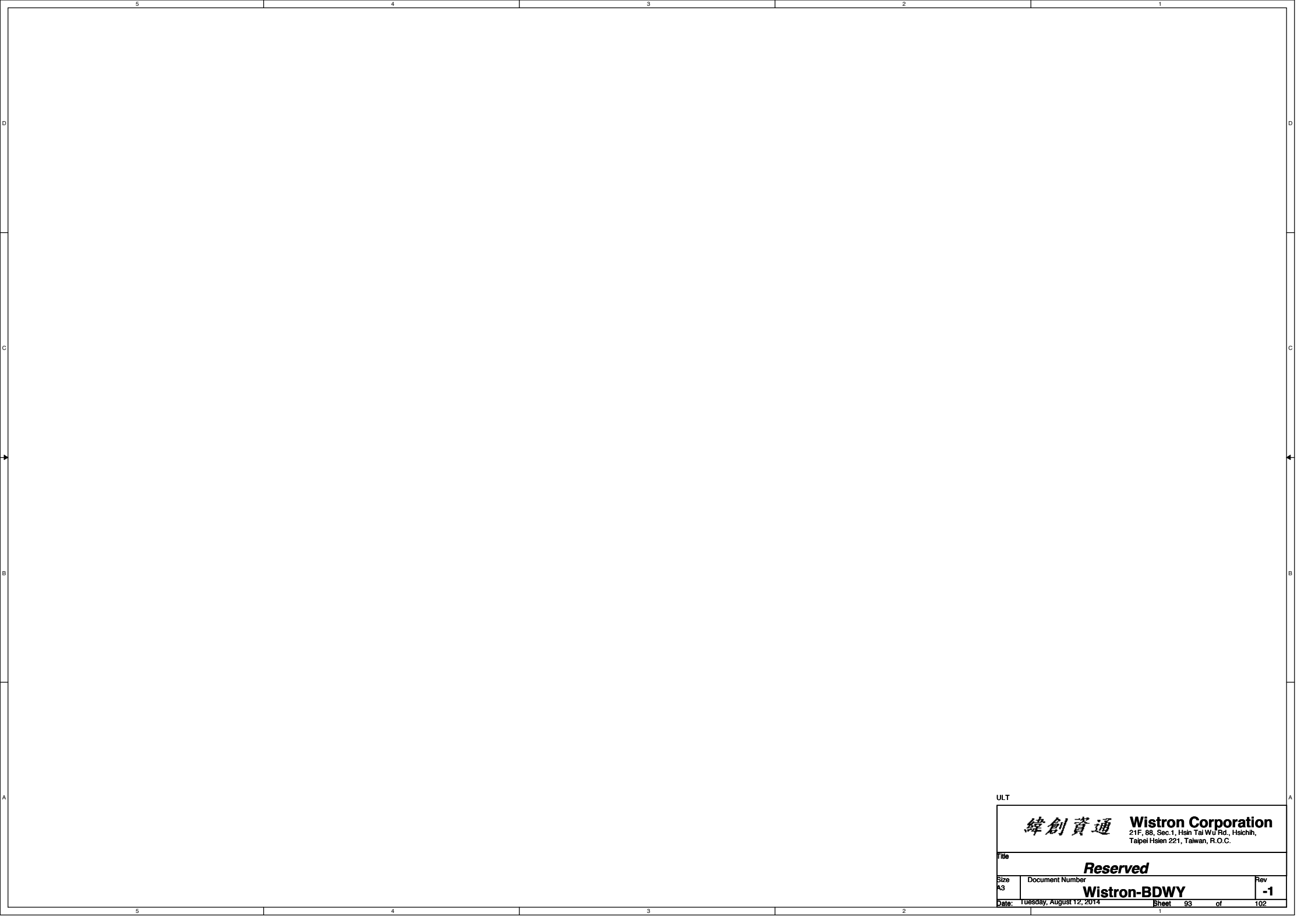
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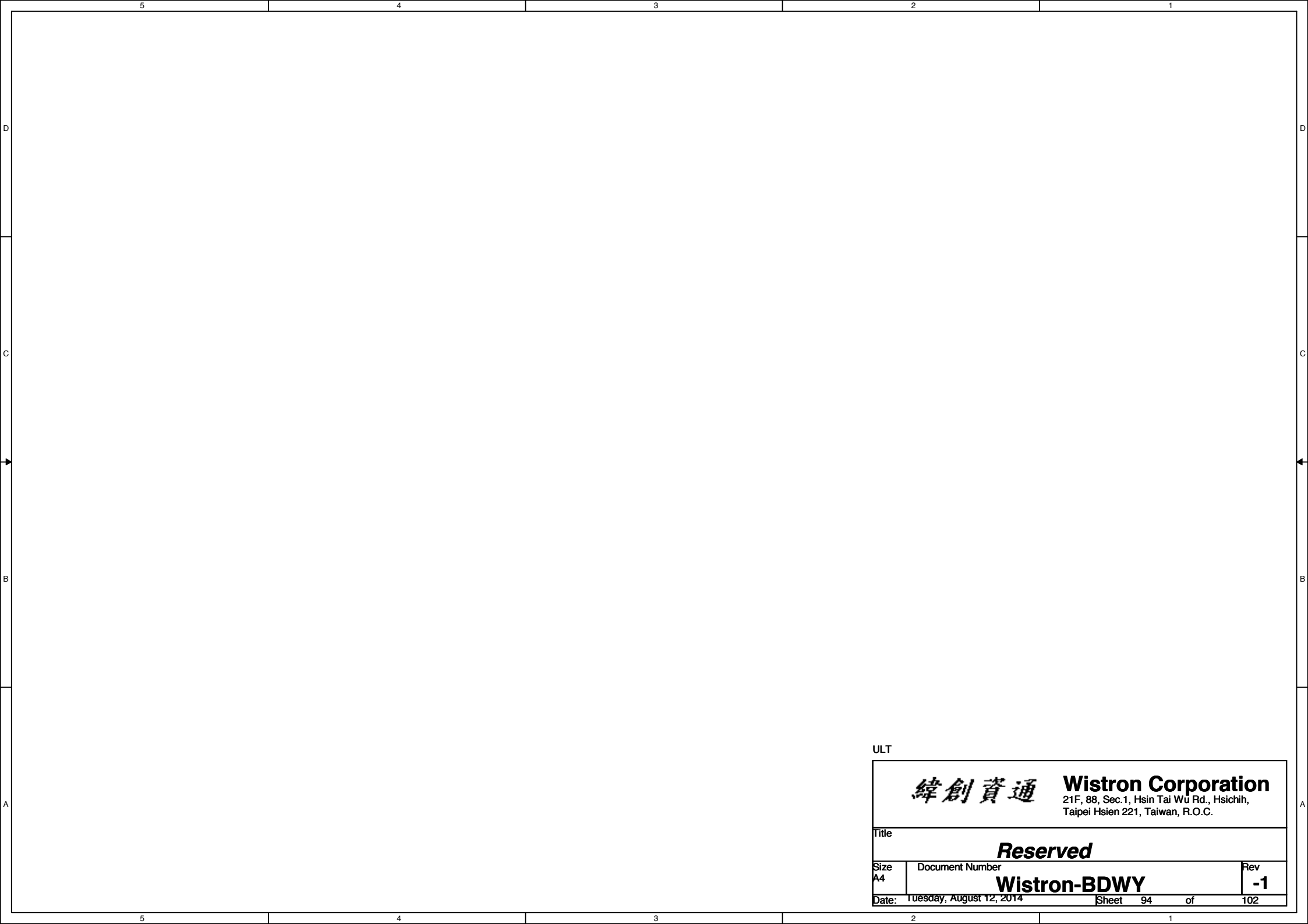
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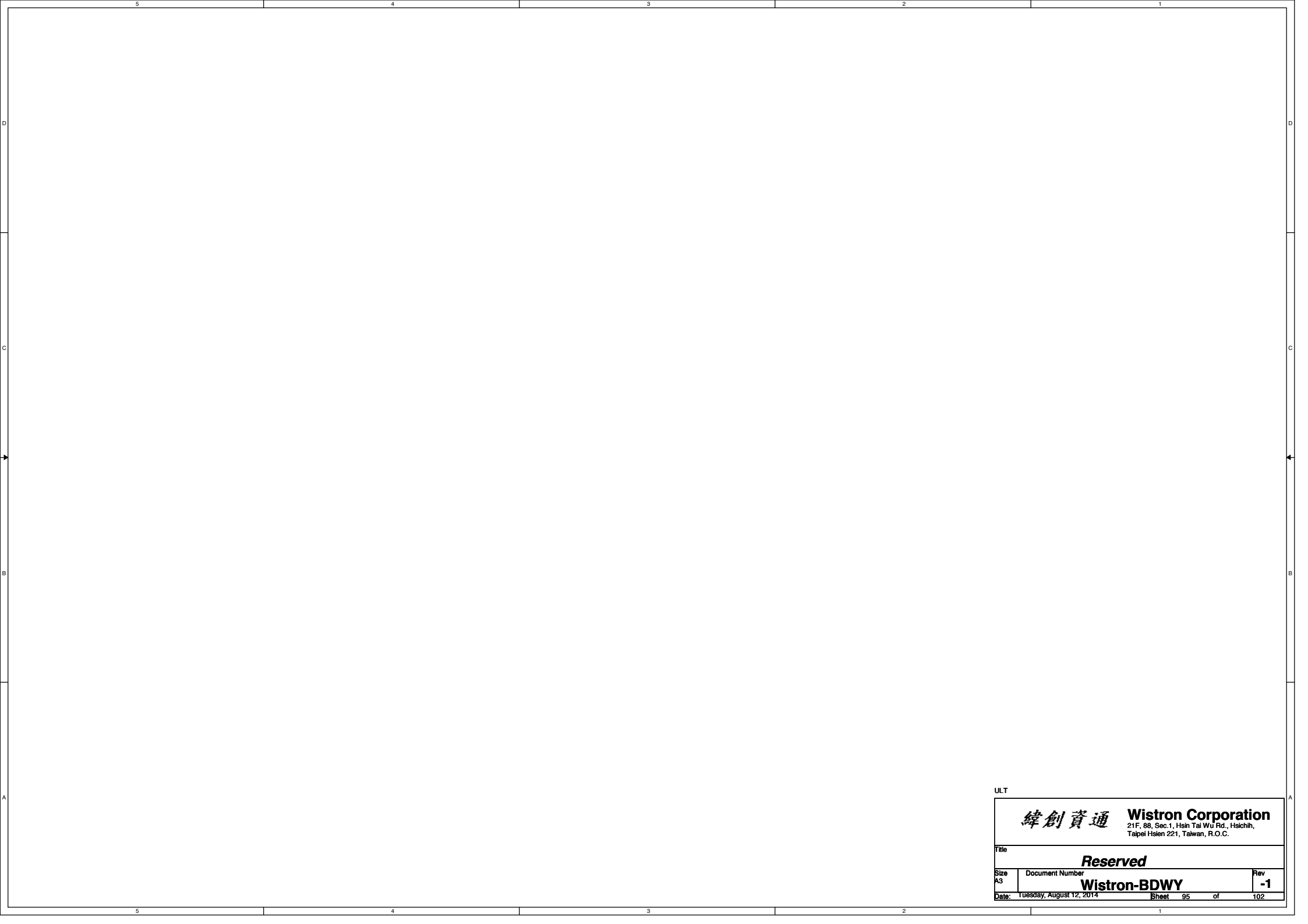
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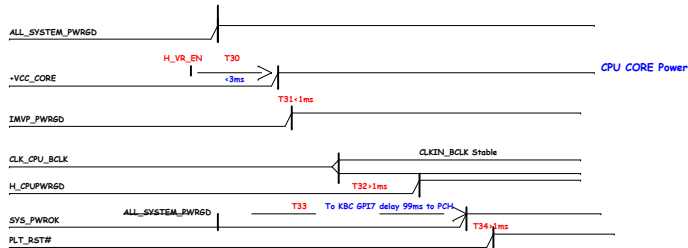
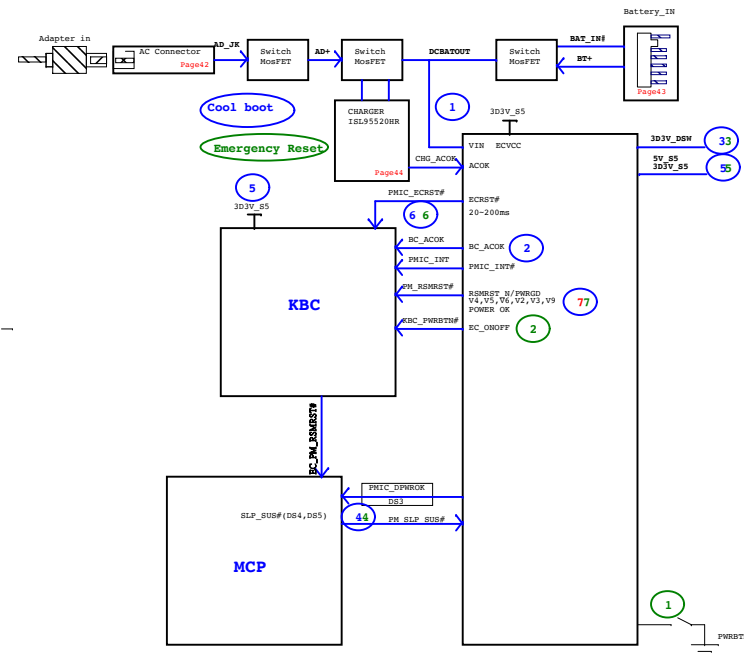
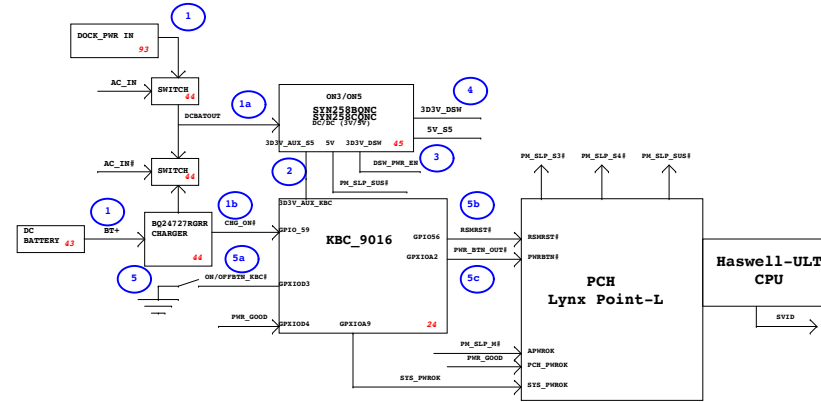
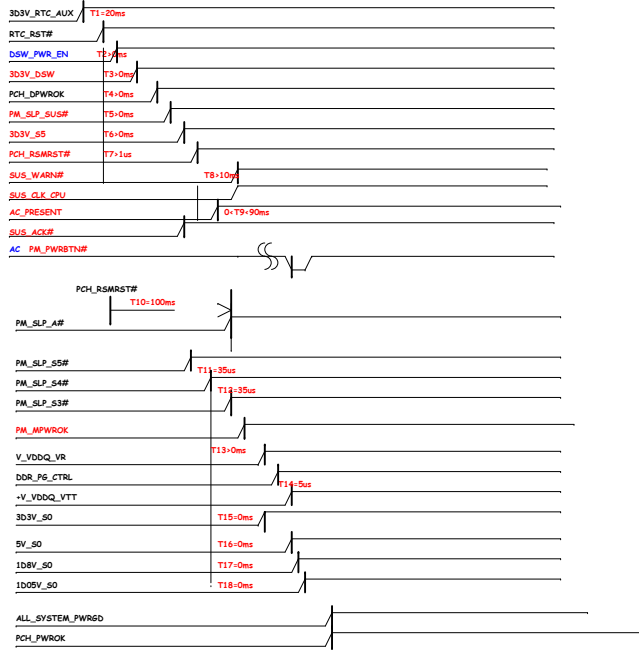
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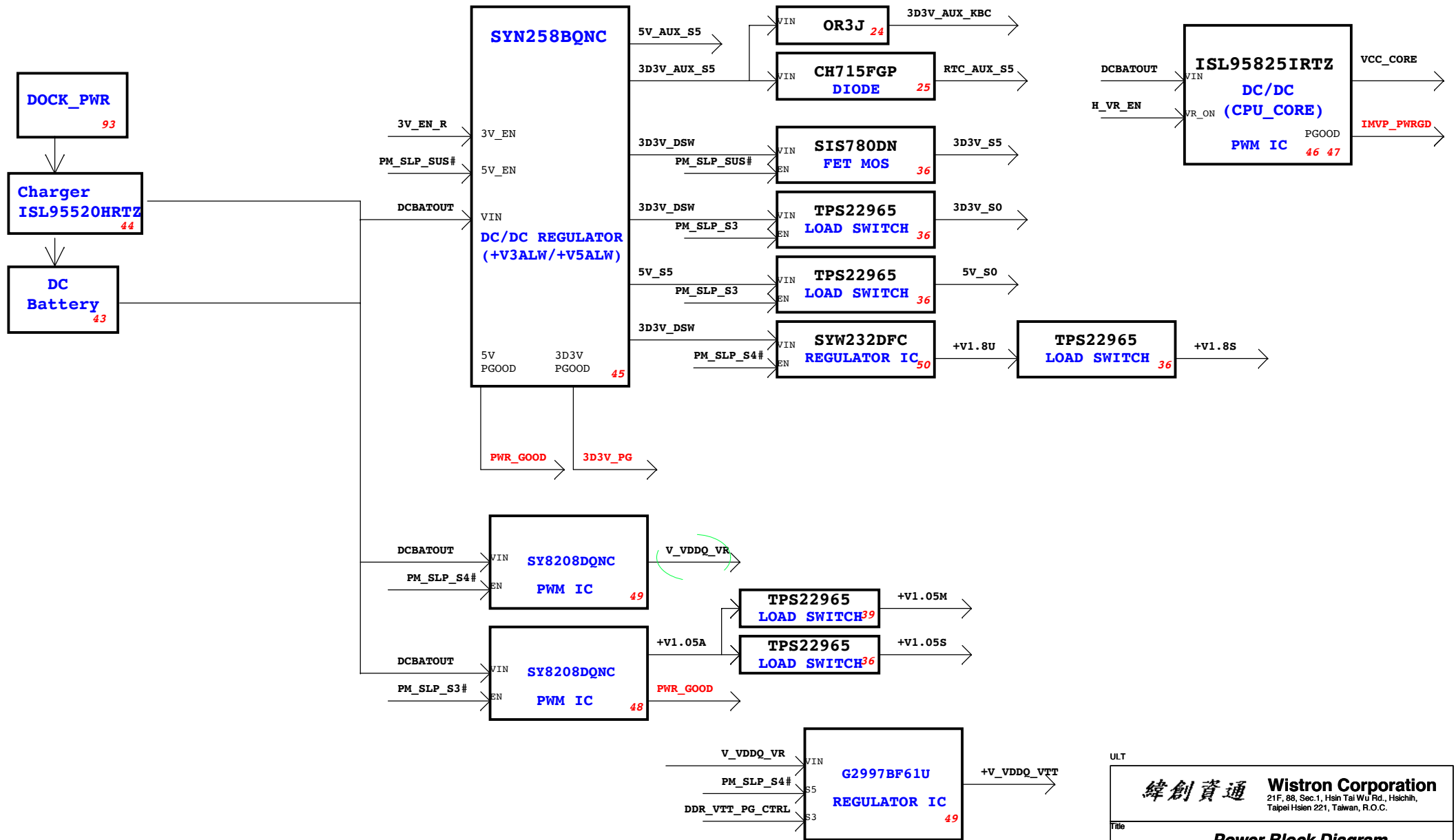
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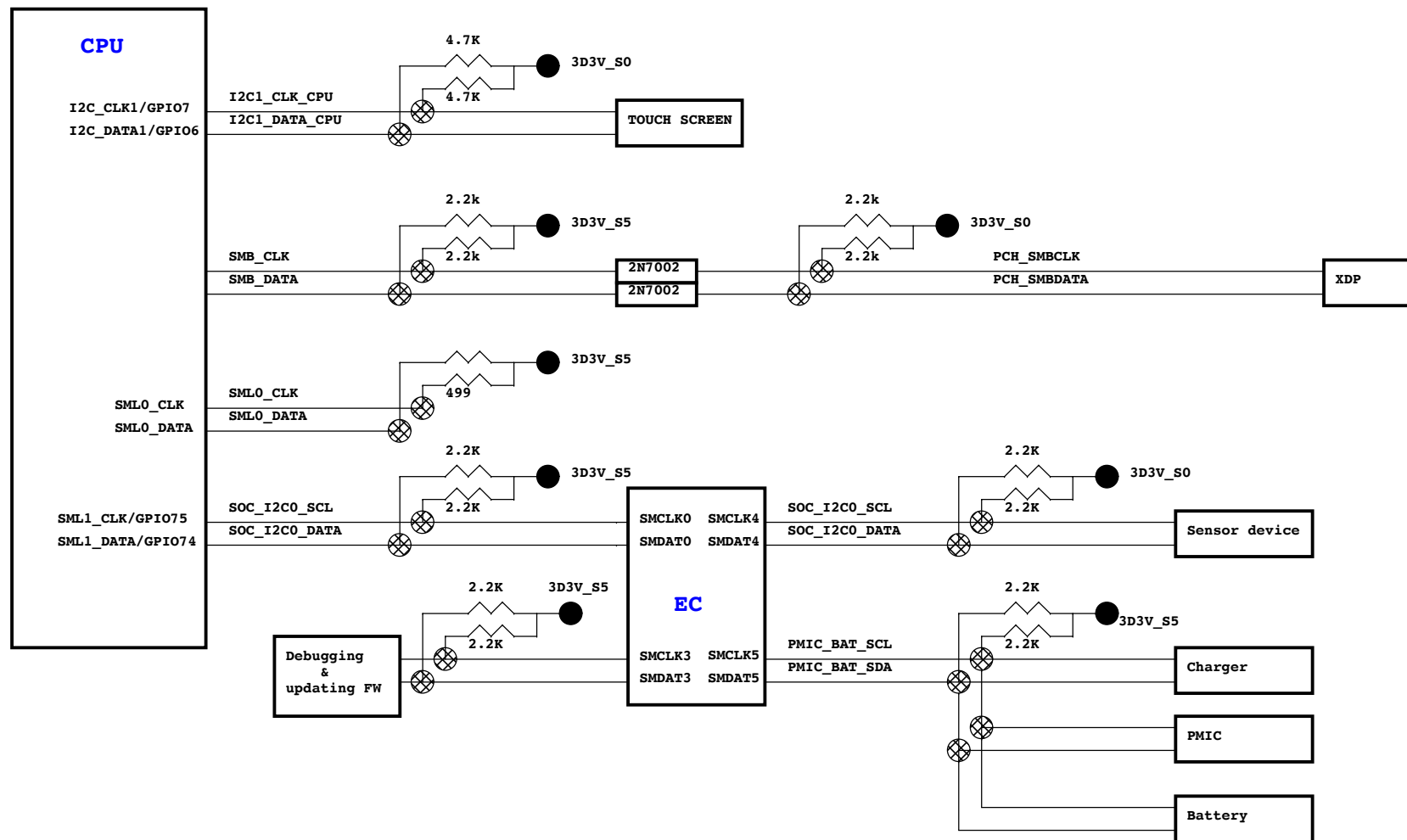
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BDWY POWER BLOCK DIAGRAM





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